

# An FPGA-based Coaxial Channel Emulator for Automated Testing and Validation

A Technical Paper prepared for SCTE by

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## 1. Introduction

RF signals propagating through the coaxial plant experience numerous impairments. These include natural attenuation, micro-reflections, ingress, and distortions. These impairments can be counteracted by the predistortion, equalization, and echo-cancellation components built into Data-Over-Cable Service Interface Specifications (DOCSIS<sup>®</sup>) devices. To assist in validating the performance of these DOCSIS devices, it is necessary to subject them to channels with varying levels of impairments. Today, impaired channels are created by building physical mockups of the hybrid fiber/coax (HFC) plant with cable, splitters, and attenuators. To date, changing micro-reflection levels, for example, requires physically swapping cables and attenuators. This physical approach to channel emulation can be impractical and time consuming when needing to test many scenarios.

In this paper, we present a *Field-Programmable-Gate-Array-based Coaxial Channel Emulator* that allows engineers to emulate reflections, channel tilt, ingress, and distortions in an automated testing framework. We show network analyzer sweeps of an actual coaxial channel side-by-side with the emulator, demonstrating close agreement between the two. This approach to testing has several benefits over traditional techniques. Since it is all-digital, tests are fully repeatable, and the channel can be reconfigured in software.

The emulator is capable of modeling channels with hundreds of meters of cable, tens of taps, and arbitrary tilt, ingress, and distortion. Replicating this with hardware would require a very large, expensive setup. The emulator provides 800 MHz of instantaneous bandwidth and has both a web-based user interface and a software application programming interface (API) allowing engineers to vary channel characteristics in real time. The system fits in a 2U rack enclosure, providing a compact alternative to cable-based emulators.

### 1.1. RF Impairments in the Coaxial Plant

Figure 1 shows a portion of the HFC plant between the remote PHY device (RPD) and the customer. As the signal travels, it becomes distorted by impairments in the channel. Some common channel impairments are discussed below.

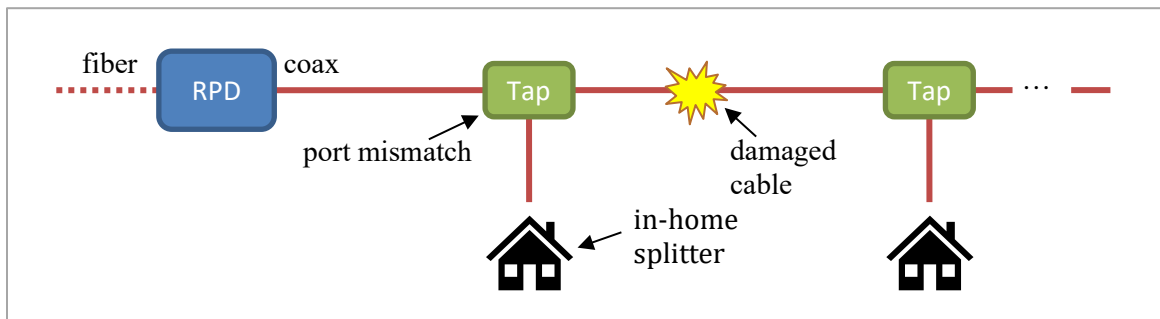


Figure 1 – Some sources of reflections in the HFC plant

**Discrete impedance mismatch** – Every interface between the coaxial cable and active/passive devices in the path causes an impedance mismatch. A cable properly terminated onto a tap may exhibit very low mismatch while a corroded ground block may exhibit a large mismatch. In each case, a reflection is generated, but in properly terminated connections, small reflections do not significantly impact system performance. Because these mismatches are electrically short (significantly less than one wavelength), they can be considered as discrete discontinuities along the cable. Sharp bends, cracks and nicks in cabling or

damaged connectors also create this type of localized discontinuity. Impedance mismatches can lead to strong frequency-selective behavior in the channel.

**Distributed impedance mismatch** – Cable damage and improperly installed connectors can allow water to enter the cable. This can cause an impedance mismatch in the cable spanning tens of feet, significantly longer than the wavelength of the RF signals traveling on the cable. This type of damage leads to distributed mismatch, which has different characteristics than the discrete mismatches discussed above. A detailed discussion of the causes and effects of water-soaked cable is found in [3].

**Nonlinearities** – Many devices in the network can contribute nonlinearity to RF signals. The most obvious source are distribution amplifiers. These nonlinearities have been studied extensively [5]. Additionally, corroded connectors creating Schottky diode-like contacts can also be a source of nonlinearity [6]. Unlike linear forms of distortion, nonlinearities lead to the generation of harmonics outside the band of the original signal, often causing interference on other frequencies.

**Ingress** – The cable network’s RF spectrum overlaps in frequency with numerous over-the-air (OTA) Federal Communications Commission (FCC) regulated bands. Cable damage and improperly installed connectors provide a path for these OTA signals to enter the network, degrading RF performance. Comcast has done extensive analysis of RF ingress power levels in different geographic areas with details presented in [4].

## 2. Modeling Channel Impairments

The RF transmit and receive electronics on each end of the DOCSIS channel have signal processing capabilities to correct for most channel impairments (this is also true for non-DOCSIS digital signals). For example, non-flat channel response due to reflections and tilt is counteracted by predistortion (on the transmit side) and equalization (on the receive side). Full duplex (FDX) DOCSIS nodes and smart amplifiers also have echo-cancellation and equalization to manage impairments due to reflections.

### 2.1. Modeling Impairments in the Lab with Coax

To test the performance of the DOCSIS channel over a range of operating conditions, channel impairments can be simulated in the lab. Several methods of simulating echoes in the lab are presented in [1]. These involve connecting lengths of cable with splitters, attenuators, and mismatches. Figure 2 shows a coaxial cable-based channel emulator that produces “single recursion echoes” and the circuit diagrams for two common coaxial emulators. The emulator in subfigure (a) is modeled by the bottom circuit in subfigure (b).

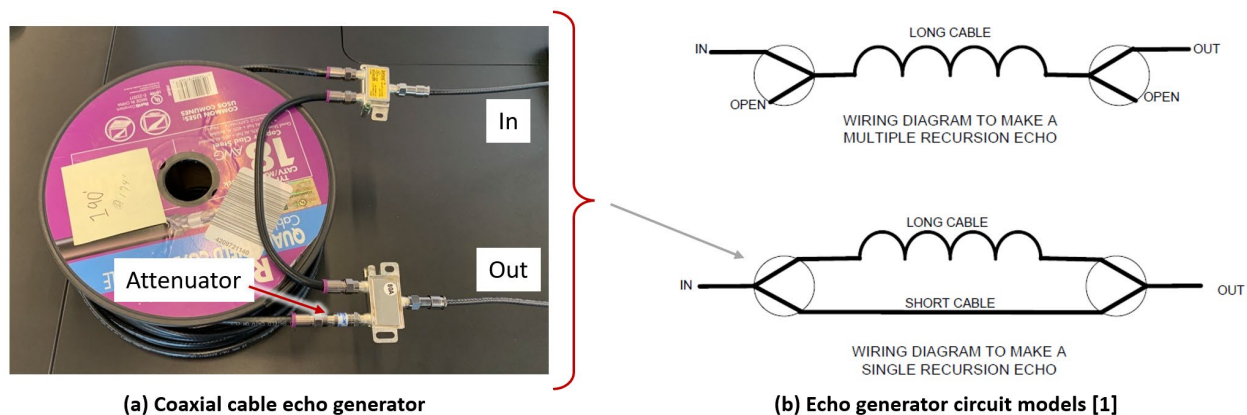


Figure 2 – Creating echoes in the lab with coaxial cable.

In the lab, a coaxial channel emulator would be physically modified by changing the length of cables or the value of attenuators to vary null spacing and depth. This process allows engineers to stress channel equalization capabilities and ensure that the DOCSIS hardware operates reliably over the expected range of channel impairments. While this approach is simple and effective when modeling simple reflections, it suffers from several drawbacks. First, the engineer must physically change components for each impairment level they wish to test. This is a relatively slow process and makes automated testing impossible. Second, cable spools are large and heavy, so emulating a full node leg would require a large, complex setup. Finally, since the emulator is composed of physical components, it is difficult to ensure repeatable testing over time and across test sites. Similarly, non-linear impairments such as a corrosion-caused diode effect have been simulated with cable and circuit boards, or actual amplifiers with bias changes. This approach is awkward and it is often difficult to tune the hardware to simulate real network conditions.

## 2.2. Digital Emulation of RF Impairments

Many challenges faced with cable-based emulators can be addressed with digital techniques. With current field-programmable gate array (FPGA) technology, it is possible to build a wide bandwidth, low latency all-digital channel emulator to model complex DOCSIS networks. In this project, we have built a prototype digital emulator around the Xilinx ZCU-111 evaluation board. The board (shown in Figure 3) contains a Xilinx XCZU28DR FPGA. This ASIC has eight analog-to-digital (ADC) and eight digital-to-analog (DAC) channels, running in excess of 4 Gsps. The chip also contains quad-core and dual-core ARM processors.

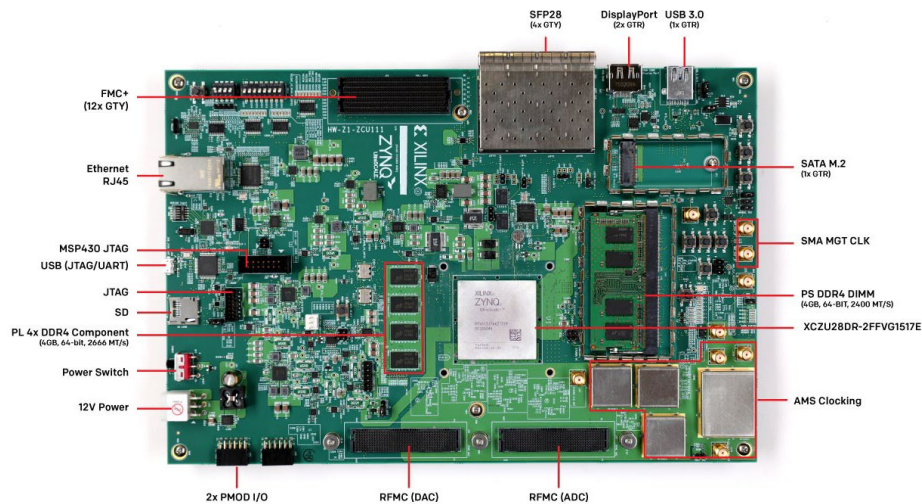
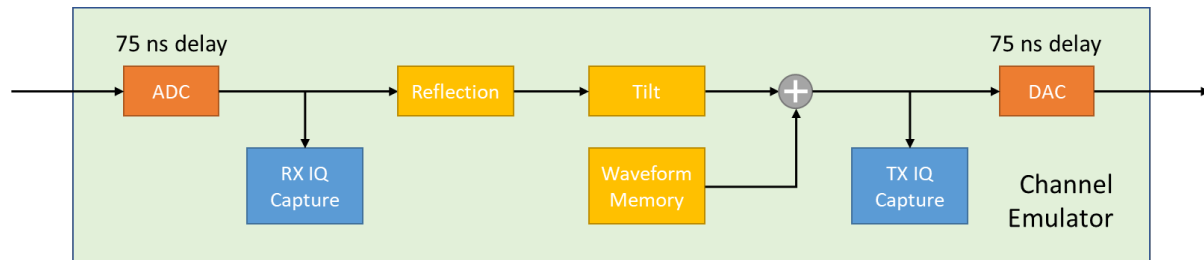


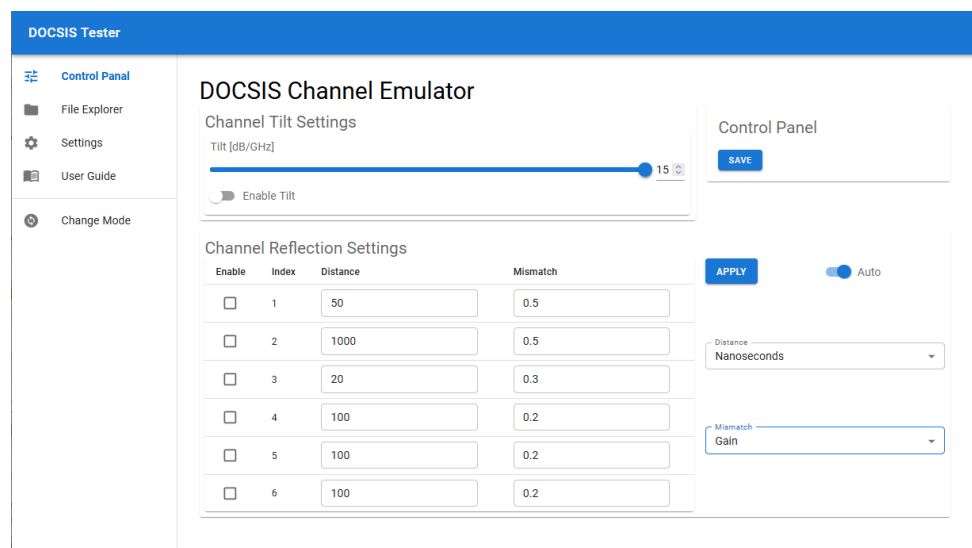
Figure 3 - Xilinx ZCU-111 evaluation board [7]

The digital channel emulator block diagram is shown in Figure 4. DOCSIS signals are digitized with the built-in ADC and converted back to RF with the DAC. The design allows the user to dynamically change the reflection characteristics of the channel and add tilt. A waveform memory allows the injection of arbitrary RF signals into model ingress. Finally, receive-side and transmit-side IQ capture modules provide real-time diagnostic capabilities.



**Figure 4 - Components of the DOCSIS channel emulator**

The FPGA's quad-core ARM processor runs Linux and hosts a web-based user interface (UI) that gives operators full control over all hardware settings in real time. The UI, shown in Figure 5, allows the operator to set channel tilt in decibels per gigahertz (dB/GHz). In the current hardware build, there are six reflection generator modules. Each is controlled by setting the distance (i.e., the length of cable) between reflections and the mismatch caused by the reflection.

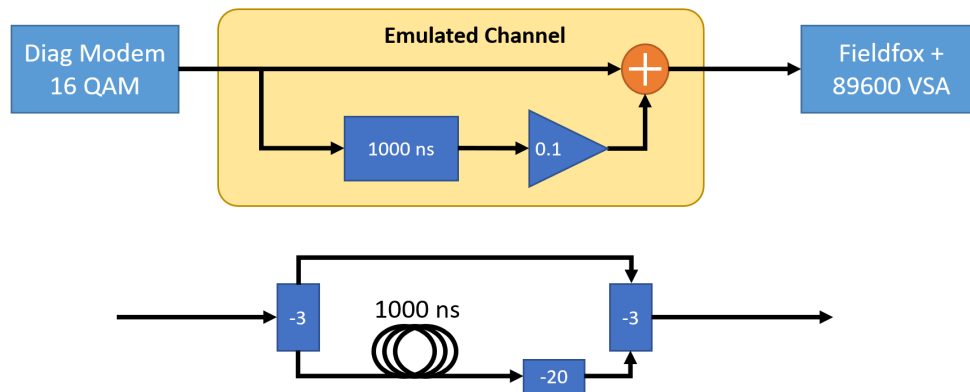


**Figure 5 - Channel emulator web-based user interface**

### 2.2.1. Emulating Channel Reflections

The six reflection modules are all identical in construction. To demonstrate their operation, we show the effect of a single digital reflection module. In the top of Figure 6, we show the hardware setup. A diagnostic modem is configured to transmit 16-QAM data continuously while a Fieldfox spectrum analyzer running Keysight 89600 vector signal analyzer (VSA) software is set to recover the data.

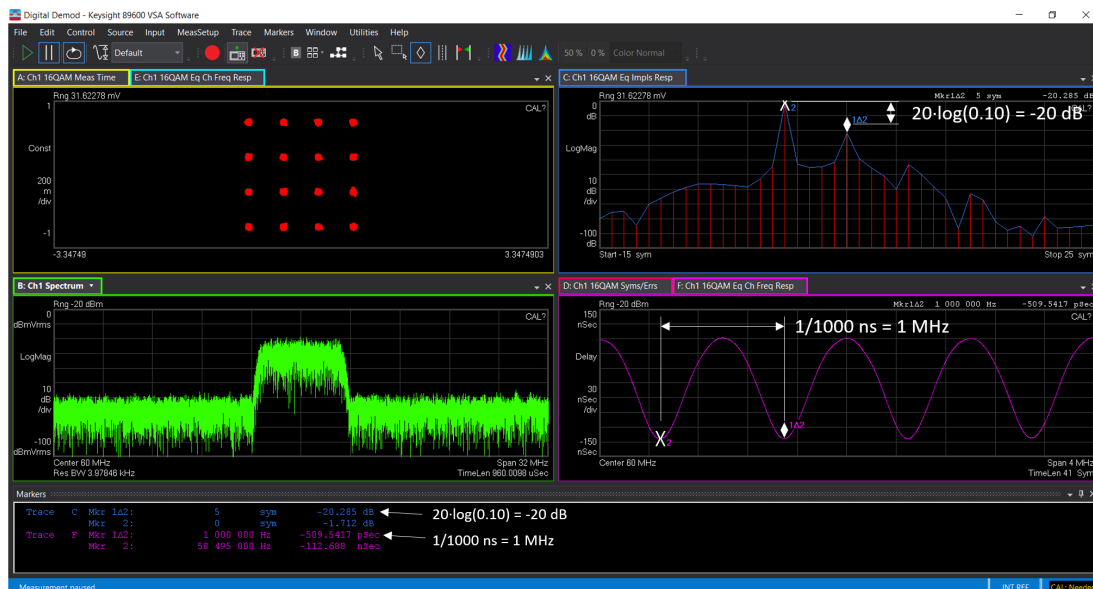




**Figure 6 - A single reflection in the channel emulator (top) and coaxial equivalent (bottom).**

Between the modem and VSA, we place the channel emulator with a single reflection enabled. The reflection works by splitting the incoming IQ signal, sending one path through a delay and attenuator, and summing the two paths. This is the digital equivalent of the *single recursion echo* in Figure 2. The bottom of Figure 6 shows how this echo would be built using coaxial cable. The delay used in this test was 1000 nanoseconds and the amplitude mismatch of the delayed path was -20 dB.

The Keysight 89600 VSA software has built-in channel equalization capability similar to that of the equalizer present in the DOCSIS 3.1 SC-QAM receiver channels. In Figure 7, we show the VSA output in response to the digital channel emulator. The top-left pane shows the 16-QAM constellation from the diagnostic modem and the bottom-left shows the spectrum of the signal. The top-right pane shows the VSA equalizer coefficients after convergence and the bottom-right shows the estimated channel frequency response.



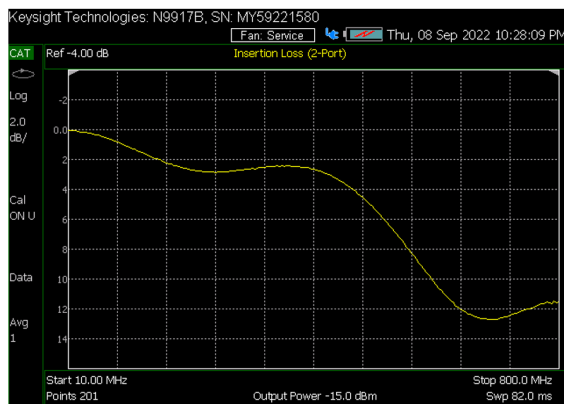
**Figure 7 - VSA output in response to digital channel emulator**

With the digital channel emulator echo path delay set to 1000 nanoseconds, we expect to see a 1 MHz ripple in the channel response. This can be verified in the bottom-right plot. Also, with a -20 dB echo level, we

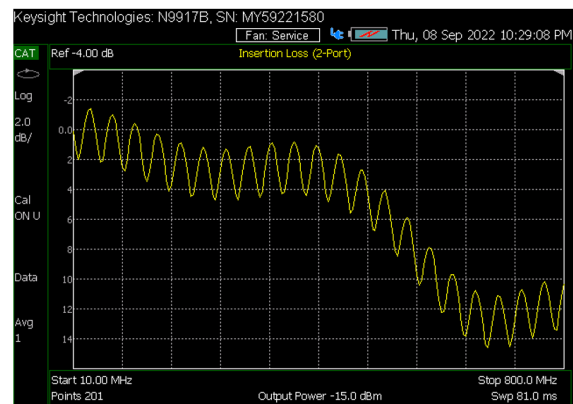
expect to see a 20 dB delta between the equalizer's main tap and first delay. Again, this can be verified in the top-right plot.

### 2.2.2. Emulating Channel Tilt

In the coaxial plant, frequency-selective attenuation leads to tilt. The channel emulator models tilt using an 11-tap programmable finite impulse response (FIR) filter. By changing the filter coefficients in real time, emulated channel tilt can also be changed. Since tilt is controlled by FIR coefficients, we are free to specify arbitrary channel frequency response curves, not just the typical constant-slope response we associate with most tilt models. Figure 8 shows network analyzer sweeps of the channel emulator with a non-linear tilt profile enabled (left) and with tilt plus reflection (right).



Tilt Enabled



Tilt and Reflection Enabled

Figure 8 - Enabling tilt (left) and tilt-plus-reflection (right) in the emulator

## 3. Other Applications of the Channel Emulator Hardware

The channel emulator is built on a general-purpose FPGA evaluation board. As such, the hardware can be designed to perform a variety of RF test functions. Two functions discussed here are *network analysis* and *wideband signal generation*.

### 3.1. Network Analysis Mode

To perform a network analyzer  $S_{21}$  measurement,<sup>1</sup> a tone is transmitted into the device-under-test (DUT) and the magnitude/phase of that tone reflected from DUT output port is measured. This process is repeated at many closely spaced frequencies to gather the complete measurement.

We have designed a bitstream for the FPGA that performs tone sweep and magnitude/phase measurement completely in fabric, allowing the emulator to operate as a network analyzer. Figure 9 shows a comparison of a Fieldfox spectrum analyzer sweep with the FPGA hardware. Each instrument was through-calibrated before testing. The right-hand figure shows agreement between the two devices of about 0.5 dB.

<sup>1</sup>  $S_{21}$  is what is known as a scattering parameter (S-parameter) for a two-port device or network, specifically forward voltage gain or forward transmission coefficient ( $E_{\text{Transmitted}}/E_{\text{Incident}}$ ). Testing a two-port device or network from Port 1 to Port 2 gives the S-parameter  $S_{21}$ .



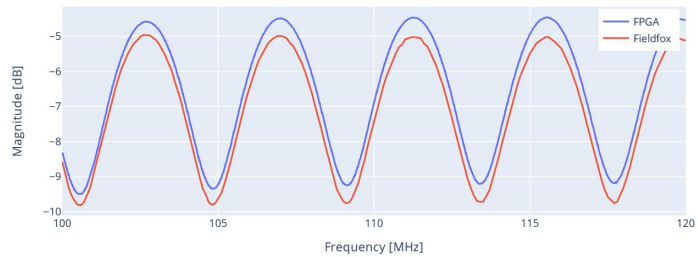
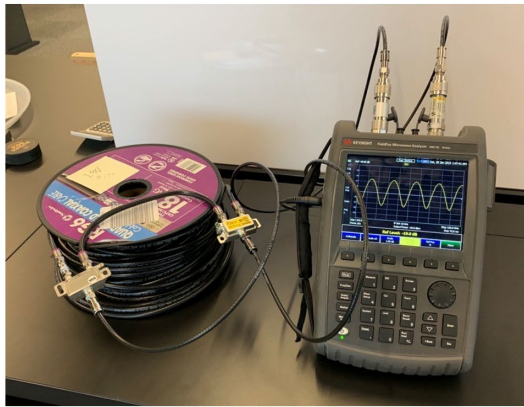


Figure 9 - Network analyzer  $S_{21}$  sweep of channel emulator

### 3.2. Wideband Signal Generation

In DOCSIS testing, it is often necessary to generate wideband signals simulating a fully-loaded spectrum. The channel emulator contains a waveform memory designed for ingress emulation, but this same capability can also be used for wideband channel loading. A mode has been added to the emulator's user interface that allows operators to specify wideband signals in terms of frequency ranges and period/duty cycle per range. The UI is shown in Figure 10.

**DOCSIS Tester**

Control Panel

PLAY SAVE

Frequency Breaks

Start Freq	End Freq	Attenuation	Pulse Group	Delete
0 MHz	108 MHz	0 dB	Off	[Delete]
108 MHz	200 MHz	0 dB	1	[Delete]
200 MHz	300 MHz	0 dB	2	[Delete]
300 MHz	400 MHz	0 dB	3	[Delete]
400 MHz	500 MHz	0 dB	5	[Delete]
500 MHz	684 MHz	0 dB	6	[Delete]

BUILD SIGNALS

Pulse Groups

#	Period	Duty Cycle	Enable	Delete
1	10 us	10 %	[Check]	[Delete]
2	20 us	10 %	[Check]	[Delete]
3	30 us	10 %	[Check]	[Delete]
4	40 us	10 %	[Check]	[Delete]
5	50 us	10 %	[Check]	[Delete]
6	60 us	10 %	[Check]	[Delete]

UPDATE

Figure 10 - User interface for wideband signal generation

Figure 11 shows a screen shot of the device producing a signal spanning 800 MHz.

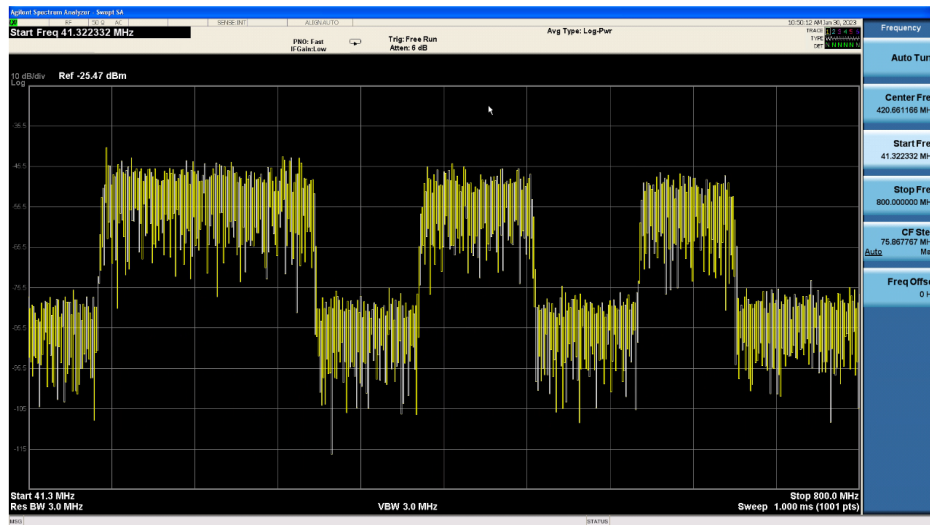


Figure 11 - 800 MHz IBW signal generation using the ZCU-111

## 4. Conclusion

In this paper, we have shown how commercially available FPGA hardware can be used for DOCSIS testing. The channel emulator allows users to dynamically create reflections, tilt, and ingress. Since this is an all-digital approach, repeatability can be achieved across test sites and testing can be fully automated. Additionally, the hardware footprint is significantly smaller than the commonly used coaxial emulators. Other common testing capabilities, including network analysis and signal generation can be incorporated into the same hardware platform, leading to a compact, low cost DOCSIS analysis tool.

## Abbreviations

ADC	analog-to-digital converter
API	application programming interface
ASIC	application specific integrated circuit
DAC	digital-to-analog converter
dB	decibel
dB/GHz	decibels per gigahertz
DOCSIS	Data-Over-Cable Service Interface Specifications
DUT	device under test
FCC	Federal Communications Commission
FDX	full duplex [DOCSIS]
FIR	finite impulse response
FPGA	field programmable gate array
Gsps	gigasamples per second
HFC	hybrid fiber/coax
IQ	in-phase/quadrature
MHz	megahertz
ns	nanoseconds
OTA	over-the-air
QAM	quadrature amplitude modulation
RF	radio frequency
RPD	remote PHY device
SC-QAM	single carrier quadrature amplitude modulation
UI	user interface
VSA	vector signal analyzer

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