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Optimizing Active Components for Extended Spectrum Networks

A Technical Paper prepared for SCTE•ISBE by

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1. Introduction

Upgrading current hybrid fiber coax (HFC) networks to extended spectrum (ES) introduces many challenges for operators, equipment providers, and component vendors. Historically upgrades have been accommodated by utilizing improved component performance to develop actives that drop into existing network locations. A drop-in strategy means minimal downtime and reduced labor costs.

Given the familiarity of this strategy it's natural to look at upgrading current actives for ES by leaning on newer component technologies to reduce costs while realizing the goals of increased bidirectional bandwidth. The extension to 1794 MHz might be difficult enough to force a departure from the standard architectures by adding additional active elements at key places in the network. However, before we get to that point the question remains: how far can newer component technology take us?

Major goals for an ES upgrade center around reusing as much of the existing active installations as possible. Ideally, system power supply capacity should not be exceeded, and active upgrading should consist of replacing old equipment trays with new ones without changing locations or re-splicing cables. To not disturb operating levels to existing customers, current output levels are maintained. Any additional energy located in upper bands must be facilitated through the use of newer, more efficient amplifier components powered from the same or lower DC power as today.

Historically, the cable industry has struggled to employ a sufficient workforce during major upgrade cycles. While client-side silicon capable of meeting the full DOCSIS 4.0 requirements may be a way off, it would be advantageous to have ES capable actives soon that are both legacy friendly and easily switched to an ES configuration. ES capable actives can then be deployed as soon as they are ready which will help smooth demand on the workforce when the new modems are ready.

The ES upgrade challenge is like increasing the link budget of a legacy communication system, much of which has been based on older component technology. The incremental losses at 1794 MHz, particularly for customers in unfavorable tap locations with lesser-grade coaxial cable served off long drops can be substantial. Rolling back the quadrature amplitude modulation (QAM) rates for these customers works counter to the purpose of the upgrade. The transmit (Tx) performance from the network active cascade and the receive (Rx) performance at the point of entry (PoE) are key parameters available to offset the detrimental effects of increased losses. In most cases today, components operating in the field provide lower levels of Tx and Rx performance compared to what is readily achievable in a new generation of components using technologies that now serve key locations in wireless networks.

Other improvements and optimizations outside the scope of this paper provide additional performance margin. Low density parity check (LDPC) codes provide distinct advantages over existing Reed Solomon error correction. Similarly, there has been much study about how to best allocate an amplifier's total composite power (TCP) capability by offsetting and adjusting the upper spectrum to 1794 MHz to best fit the physical plant realities.

This paper focuses on how Tx and Rx performance at key locations in the network may be improved to smooth the path for the emerging ES upgrade. In particular, the design methodology for a new set of components targeting optimum Tx power under a fixed DC budget for an ES line extender (LE) is presented. We propose a multiple-stage integrated-circuit-based design approach to optimize overall performance. Likewise, achievable Rx performance is shown as an opportunity for point of entry (PoE) devices.

2. The Importance of Bias

Class A amplifiers have served the cable industry well. They provide a good combination of bandwidth and linearity necessary to handle legacy analog TV encoding. Fortunately, networks have been upgraded over time to maintain the high level of linearity needed for analog signals, which serendipitously makes them excellent candidates for handling high level QAM signals in the high bandwidth digital era.

Of course, the downside of Class A stages is their poor efficiency. Achieving high linearity takes a lot of DC bias. Amplifier crash point, the RF output power level where modulation error ratio (MER) rapidly falls as input drive is increased, is likewise dominated by biasing considerations. Although methods of linearization, such as digital pre-distortion (DPD) and legacy analog pre-distortion can provide worthwhile benefit, ultimately crash levels and the ability to increase Tx TCP levels are still constrained by bias. Once a transistor runs out of voltage or current as it traverses along its load line it is no longer capable of reliably carrying information.

It follows then that to maximize the Tx TCP performance attention should be focused on how to optimally allocate bias in the cascading component stages. Higher TCP levels are usually within reach, as demonstrated in recent fiber deep output stages, but at cost of additional DC power that probably eclipses the available legacy power of a high percentage of the networks operating today.

There are any number of ways to adjust bias conditions in Class A amplifiers. The most common and obvious involves adjusting the quiescent current of the stages within a design. However, as equipment vendors seek to differentiate their offerings, it's worthwhile to note that an additional level of efficiency is available by incorporating the supply voltage as part of the design optimization. On this point many vendors have been inflexible on supply voltage and consequently left performance on the table to their competitive disadvantage.

Table 1 highlights the costs and benefits of a few examples of bias control schemes. As ES amplifiers emerge, greater thought can be given to the benefits of incorporating a network management system (NMS) as part of an intelligent network. The techniques below are not mutually exclusive and may be combined to innovate equipment designs. Here the term "bias" is inclusive of both voltage and current being applied to an amplifier component.

Table 1 – Examples of Bias Control Schemes

Technique	Description	Advantages	Disadvantages
Factory / Field Bias Set	Adjust once and forget	Low cost	Inflexible
Active Bias Control	Localized control loop	Minimizes variations unit-unit and over temperature	Minor cost adder
Remote Bias Adjustment	NMS monitoring and control	Configurable to network differences	Added cost
Automatic Bias with Static RF Level	Servo based on required or NMS controlled RF level	Ease of deployment and optimized efficiency	Added cost

Technique	Description	Advantages	Disadvantages
Envelope Tracking	Dynamically adjust based on derived signal envelope	Significant improvement in efficiency	Must know envelope condition and have means to suitably adjust bias conditions, cost of added circuitry
Active Linearization	Dynamically adjust based on full spectrum of input signal	Significant improvement in efficiency	Requires much higher speed device processes

3. Introduction to Design of an ES Line Extender

3.1. Legacy 2-stage Line Extenders

To help with the bias optimization process for ES line extenders, we considered the interaction of gain, corresponding RF output level, and bias expenditure of a hypothetical LE design. For a given RF input level the amount of gain in a stage is intimately connected with its RF output level requirement. We considered how we could develop a family of amplifier components that would optimize cascaded LE performance while fitting within the legacy power available in today's line extenders. By carefully distributing the amount of gain and bias in intermediate stages we sought to maximize bias available for the final Doubler stage, thereby hoping to maximize the Tx TCP and MER budget.

Of course, line extenders have additional loss elements in the RF path, such as diplexers, automatic gain control (AGC) circuits, directional couplers, and tilt equalizers. Since one goal is to maintain legacy levels in an ES deployment the amount of tilt needed considerably rises. Because most of the tilt is accomplished with passive circuits the cascaded gain must be increased. In addition, the location of this tilt loss must be carefully considered since it places added burden on both the cascaded noise figure and distortion performance of the line extender.

As a starting point, consider a simplified downstream LE block diagram in Figure 1. Two stages of amplification are commonly used in most line extenders today. Depending on how RF output level control is implemented, downstream LE gain for a 1002 MHz design ranges from 39 to 33 dB. An input "Push-Pull" and an output "Doubler" combine to provide approximately 48 dB of amplification. Interstage losses account for the difference between total LE gain and gain provided by these amplifier components.

Cascaded tilt in the range of 8 to 18 dB are commonly configured by applying appropriate tilt modules. Locating most of the tilt directly at the input will deteriorate overall MER performance through thermal noise mechanisms. However, distortion contributions to MER performance will be minimized since each stage operates with a high input tilt. Conversely, locating most tilt between gain stages leads to MER degradation from the driver amplifier since it must drive a higher RF level through the tilt loss.

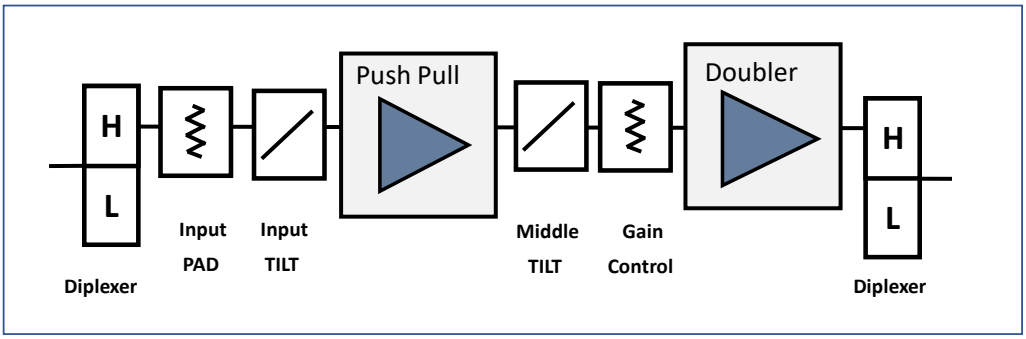

Figure 1 – Simplified Downstream Line Extender

To overcome the additional plant loss in an ES buildout, LE gain must be increased by as much as 16 dB compared to legacy 1002 MHz line extenders. Operating tilts will naturally increase to around 22 to 26 dB, meaning that thermal noise contributors to MER degradation will be more difficult to manage. Add to this the desire to carry high levels of QAM in longer RF cascades such as N+4 or N+6, and the problem of where to locate the additional gain and tilt becomes non-trivial.

3.2. Gain Limitations in Single Stage Amplifier Components

Most gain stages in cable networks use the familiar cascode topology in a push-pull configuration. Figure 2 shows the familiar single stage cascode topology. We consider a cascode a single stage amplifier since feedback is wrapped around both transistors in the configuration. A combination of series (RS) and shunt feedback (RF) is used to set impedances and manage gain flatness. Due to limitations in intrinsic transistor transconductance and bandwidth, gains of single-stage 1800 MHz amplifiers max out around 23 dB. However, in our testing a slightly lower gain 21.5 dB version has shown superior efficiency performance.

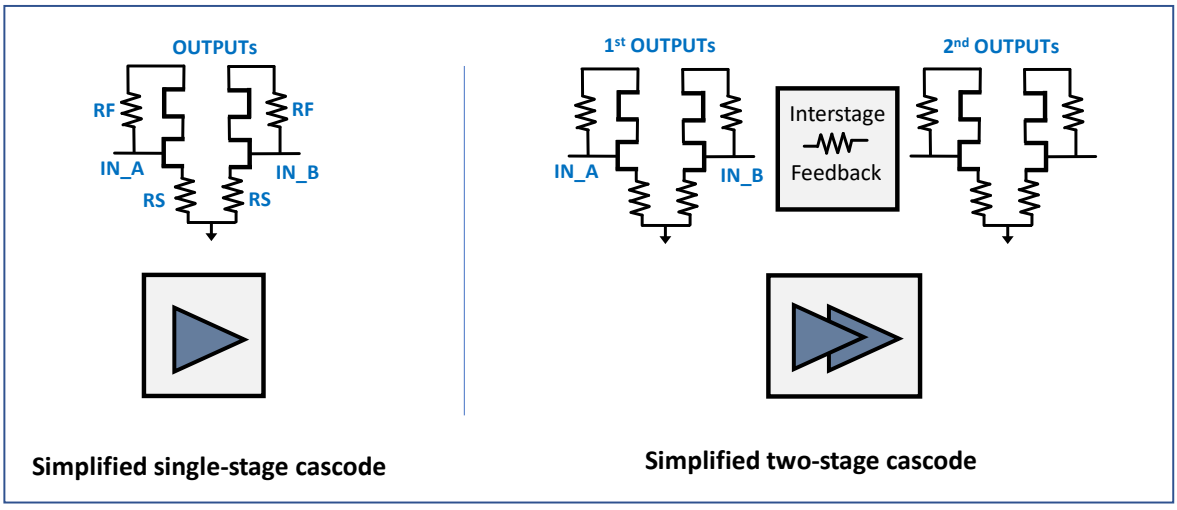

Figure 2 – Single and Two-Stage Cascode Amplifier Component Topologies

For intermediate level designs using simple baluns on the input and output, practical gains are closer to 19 dB per stage. These devices commonly take a reduced 5 V to 8 V supply voltage and output a suitable level to power moderate amounts of attenuation and tilt leading to the output Doubler stage. Because these designs have lower power consumption, they can be fabricated on a single die leading to more

consistent performance. If standard baluns are used for unbalanced-to-balanced conversions designers can achieve good impedance consistency using little board space. Standard GaAs processes are commercially available to fabricate these circuits leading to acceptable overall cost.

3.3. Two Stage Design for Additional Gain and Negative Feedback

Figure 2 also shows a two-stage cascaded cascode amplifier component concept. The additional stage provides a boost in available gain useful in any number of additional series or shunt on-die feedback arrangements. This provides the integrated circuit designer freedom in setting impedance over a wide range of gain levels. It's possible to design a two-stage integrated circuit where fabricating a range of gains is just a matter of changing on-die resistor values. Practical gains for this two-stage approach range from 22 dB to 30 dB.

An example of a single-die two-stage 25 dB gain design with moderate interstage feedback is shown in Figure 3. The high degree of feedback provides consistent performance over temperature and fabrication process variations. Gain stability over temperature for the 25 dB prototype inclusive of input and output baluns is shown below. Bias current variation over temperature was +/- 1.5%. Data was taken from a heat sink temperature of -30 deg C, 25 deg C, and 100 deg C.

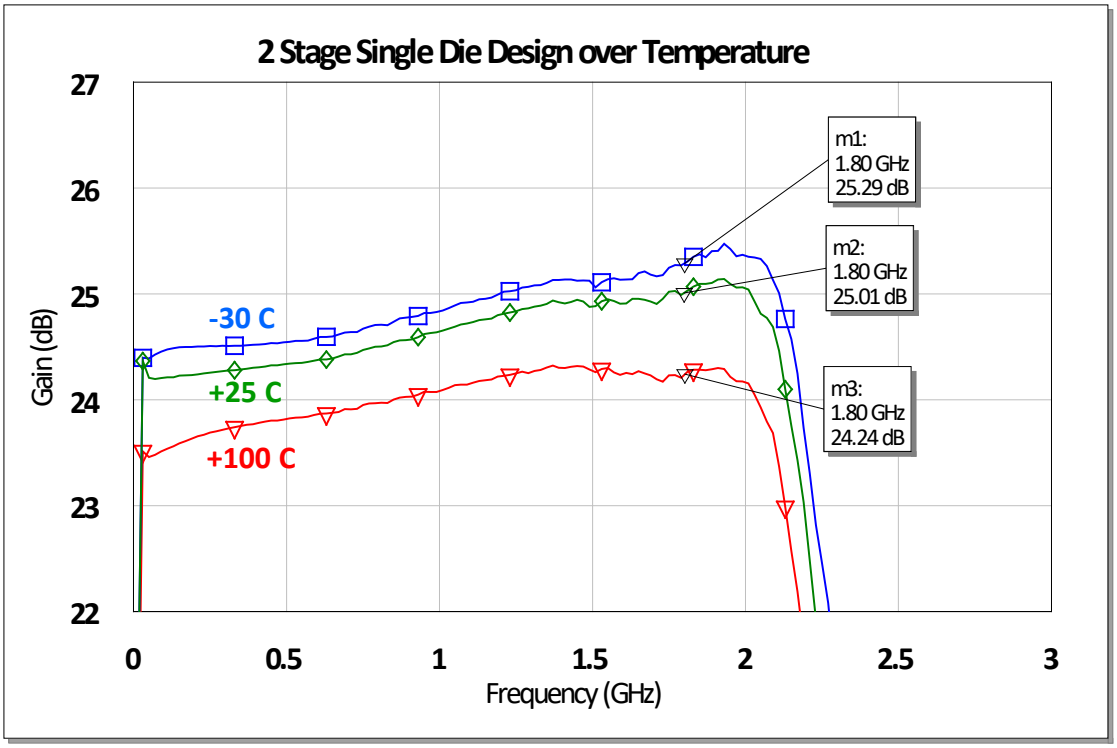

Figure 3 – Two-Stage Gain over Temperature

3.4. Common Packaging, Pin Definitions, and Application Artwork

In many cases developers of equipment need flexibility to adjust their designs with different gains and power levels to serve the wide range of operator requirements. In the past component vendors relied on the SOT115 package to offer different gain levels to the market. By leveraging this approach, we can

design single stage and two stage integrated circuits with a common application circuit and layout. A bill of materials (BOM) change is all that is needed to adjust gain and DC power consumption levels.

For example, an industry standard 5mm x 5mm QFN package with an exposed backside paddle can be used to package a family of intermediate level amplifier components, with gains ranging from as low as 12 dB through 30 dB. With good thermal precautions, power consumptions of up to 4 W can be managed easily, although as will be seen later our initial integrated-circuit designs consumed between 1.7 W and 3.0 W.

3.5. Options for Higher Gain in Line Extender Design

With available gain levels from components in mind, a few options for implementing higher gain can be considered. The question becomes how to optimally achieve the higher gain with additional stages in a modified LE block diagram while holding to the power envelope. A few options are shown in Figure 4.

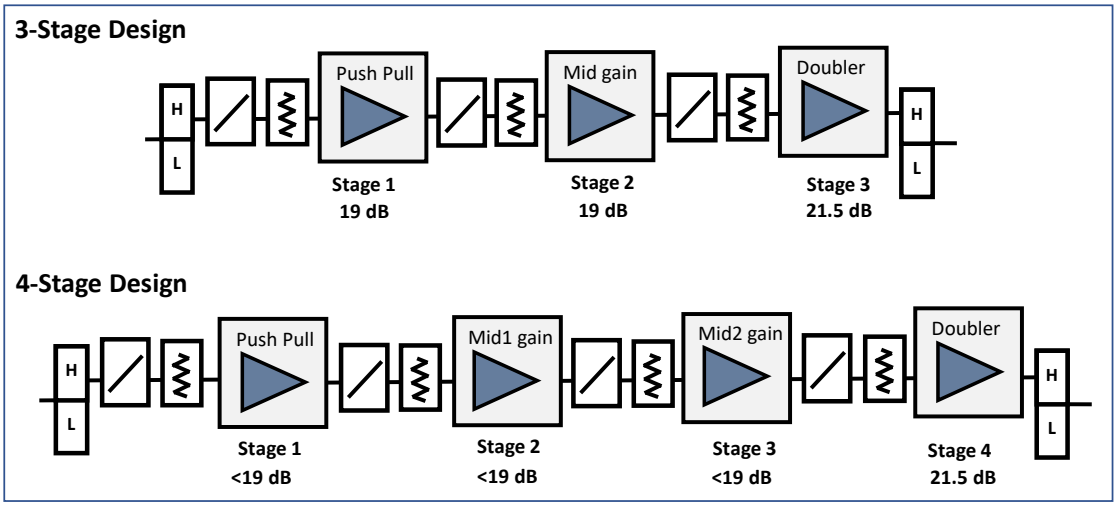

Figure 4 – Options for Increasing Downstream ES Gain

A 3-stage design utilizes push-pull and mid-gain stages operating from the lower supply rail which provide up to 19 dB of gain. Tilt and gain control can be accomplished in any number of ways with variable loss circuits to optimize dynamic range. An output Doubler provides up to 21.5 dB of gain. Although simple enough, the 3-stage design will struggle to provide enough gain to serve the entire range of LE gains operators need to drive a wide range of physical plants currently in service.

A 4-stage extension provides good gain, allowing design margin to locate interstage attenuation and tilt networks for best station performance. However, the added cost of the 4th stage is a disadvantage considering the anticipated cost pressures on LE upgrade modules.

An alternative is found in a 4-stage design, implemented in 3 amplifier components, termed a 3a stage design in Figure 5. Here the middle stage is a single die design encompassing 2 cascode stages with feedback wrapped within the 2 cascode stages.

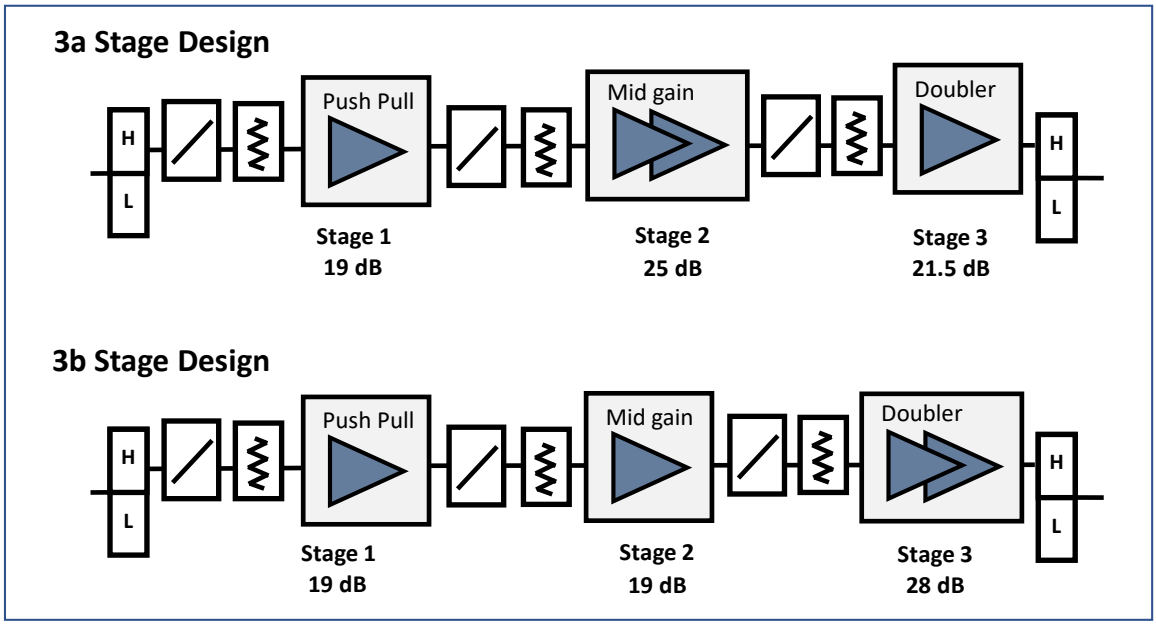

Figure 5 – High Gain 3-Stage Design Options

3.6. Variable Attenuators

Gain adjustment can be performed using variable attenuator circuits around the various stages. Since gain of the line extender can shift from unit to unit and over temperature, variable attenuation is commonly used to adjust for these changes. Maintaining a flat frequency response and consistent return loss over a moderate range of attenuation is of primary importance to reduce cascaded frequency response ripple. Unfortunately, in attenuator design there is often a tradeoff between impedance consistency over attenuation, attenuation range, and minimum attenuation. Traditional approaches have considerable insertion loss while newer designs have less. Because there are a wide range of implementations used by equipment vendors it behooves manufacturers of amplifier components to provide a wide range of gains in a common package and footprint to provide equipment designers the flexibility necessary to reach their goals.

4. Empirical Modeling Work on Early Devices

Given the interplay between gain, bias consumption, and output level capability, we sought to construct a measurement-based representation of early prototype 1800 MHz capable devices for use in LE system simulations. We fabricated standard cascode topology push-pull amplifiers on a single gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) die with series and shunt feedback resistors chosen to achieve close to the high end of realizable gain comfortably beyond 1800 MHz. Single-stage and two-stage designs were fabricated. With a single-stage 19 dB gain intermediate level stage as a starting point, we characterized the relationship between bias current and voltage, MER, output TCP level, and various tilts. Our test source exercised 384 to 1794 MHz with a 6 dB offset above 1026 MHz

Tilt, voltage, and current were exercised extensively to produce a comprehensive data set for these devices. We then developed an interpolative software model for this device which could be used for

continuous simulation of gain and linearity within the bias and tilt space of the original data set. The data collection was thorough enough that the model very closely matches actual device performance. Figure 6 shows an example of output from the device model over a range of bias and output conditions.

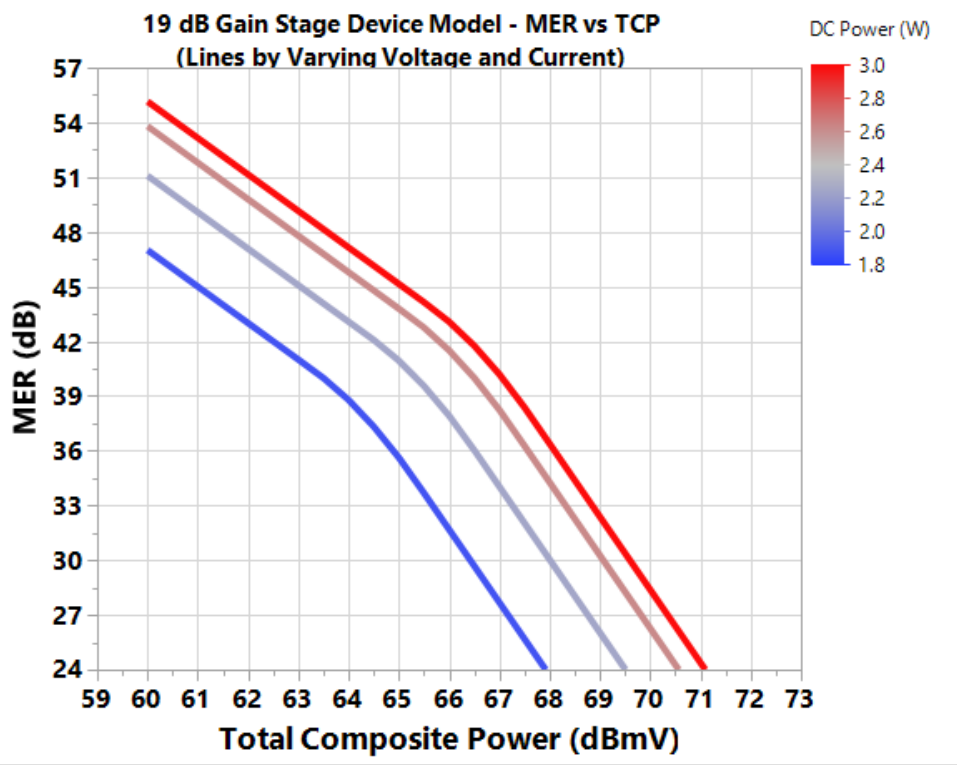

Figure 6 – MER Modeling Example

We also fabricated early devices for building output Doubler stages. We intentionally kept the question of supply voltage(s) open, knowing that this choice has major ramifications on overall TCP performance and efficiency outcomes. While historically a 24 V rail has been a strict requirement on Doubler output stage designs, the evolution of device technology has opened possibilities for improved Doubler performance using non-24 V rails. Recent 34 V Doublers serving the higher TCP Fiber Deep architecture are one example of what can be achieved with a wider design window. Furthermore, we assumed that the optimum LE TCP efficiency would come from two distinct supply rails – a higher voltage rail for the output Doubler and a lower rail for all other actives in the LE, including upstream gain.

Using the same approach as the 19 dB gain stage, we characterized the 21.5 dB gain Doubler stage and developed a model for use in system simulations.

5. Optimizing Gain, Bias, Tilt, and AGC Allocations

5.1. Cascade Simulator Concept

Equipped with models for extended spectrum active devices, we set out to develop a model for a complete LE. The intent was to determine the guiding principles for choosing the optimal topology for an LE, including the distribution of gain, tilt, biasing, and placement of any AGC element(s) or other lossy elements. This would both inform the development of a more comprehensive portfolio of extended spectrum active devices and allow us to provide data-supported recommendations for LE layout and

design. In order to extend our active device models into a full LE simulator, we had to develop several additional elements. First, simple passive element models (diplexers, equalizers, plug-in attenuators, and variable attenuators) were developed. Second, bounding conditions and assumptions on passive elements for LE design had to be determined. Lastly, a tool capable of cascading the system had to be developed to work with these models. In order to operate with the non-standard device models, we had developed for the active devices, we chose to create a custom cascade simulator for this purpose.

Starting from a defined un-tilted input and a perfect SNR, the simulation tool operates on an arbitrary topology of LE passive and active elements, cascading MER, noise, and signal in the downstream path. The cascade technique assumes that the MER can be treated as equivalent to uncorrelated noise power for the purposes of cascading. We found this relationship can be practically demonstrated on a test bench. This model does not consider BER; however, the output levels of the active devices in a typical line extender should keep bit errors from becoming a concern for purposes of these simulations. Further, the use of higher modulation orders in OFDM carriers in DOCSIS 3.1 / 4.0 deployments results in BER which is highly correlated to MER and generally not a function of device crash behavior.

We largely focused on simulations of 3-stage topologies, as it quickly became apparent that by leveraging higher gain intermediate stages as outlined above, four active stages should not be necessary except perhaps in the most extreme high-gain, high-loss cases. Even with higher gain early stages, two-stage designs are impractical for all but the highest gain actives and lowest gain requirements for LE modules.

Except where otherwise noted, most simulations were performed for an overall LE gain window of 40-50 dB with the following constraints and assumptions:

- 70 dBmV total composite power at LE output
- > 45 dB MER performance of full LE
- 26 dB output tilt from 54-1794 MHz (24 dB passive tilt, 2 dB from active components)
- 0 dB input tilt
- 2.5 dB loss at both input and output for diplex filters and other passive elements
- 5 dB (or alternatively 3 dB) minimum insertion loss for a well-matched variable attenuator circuit
- Variable attenuator nominally set 6 dB above minimum to accommodate up to 5 dB gain loss for extreme temperature excursions (+1 dB for safety)
- 1.5 dB minimum insertion loss for equalizer/tilt modules
- ~18.5 W total DC power for downstream amplifiers

5.2. Optimizing Variable Attenuator Placement

The first question that we addressed was how to distribute attenuation – namely the placement of variable attenuator(s) as part of an AGC scheme. These could in theory be placed anywhere in the chain, but the practical locations would be between the first and second stage, between the second and third stage, or both with the attenuation split in some manner. The simulation was conclusive on this point – as long as other components are chosen and located properly, the optimal choice is to place any variable attenuation between stages 1 and 2. This keeps the output of the second stage from being overtaxed, and any noise floor concerns are better alleviated by moving a portion of the tilt after the second stage instead of shifting attenuation. This also lowers the overall gain requirement from the actives by a reasonable amount (compared to a split attenuator design). Consider Figure 7, which shows three optimized topologies for a 45 dB gain line extender, with the attenuation distributed as outlined above. Note also that the “Evenly Split” configuration additionally requires several dB more gain from the actives.

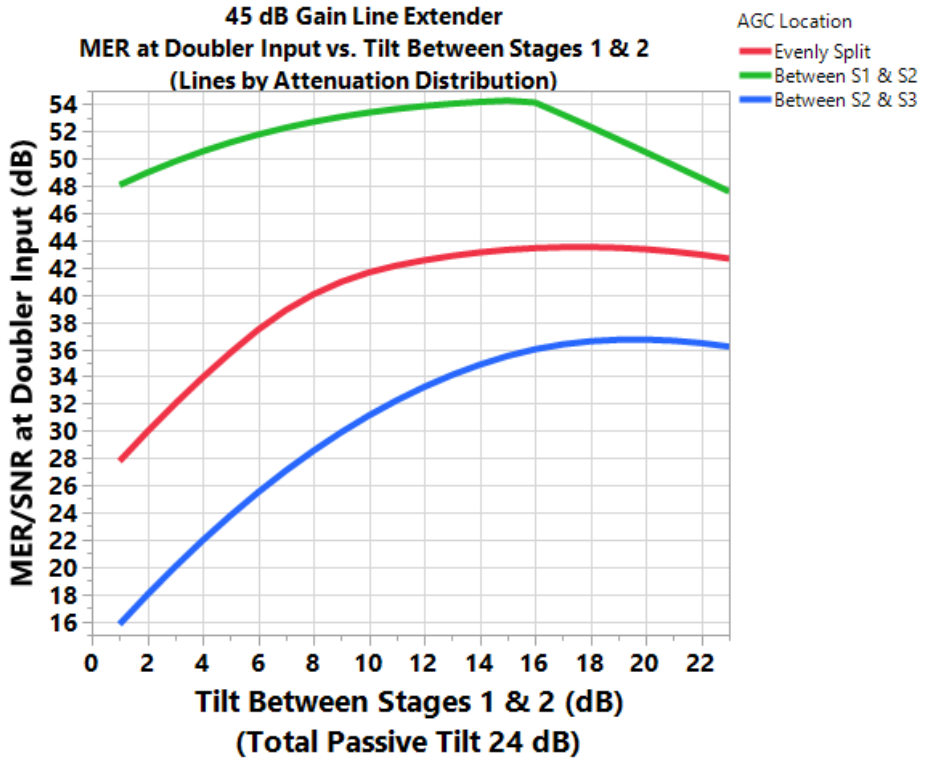

Figure 7 – Effects of Attenuation Distribution

This result fits with expectations: regardless of the distribution of attenuation, the output from the first stage remains the same. The only device linearity concern that can be addressed is the second stage's output power requirement. Optimally 100% of the attenuation and loss would be between stage 1 and stage 2 for this reason, but noise-related effects preclude this, so we seek to strike a balance by placing all of the attenuation and the "right" amount of tilt between stage 1 and stage 2.

We found that a useful metric for comparing various configurations was to look at plots of the MER/SNR coming in to the Doubler versus the amount of tilt placed between stage 1 and stage 2. The remainder of tilt is then implied to be between stage 2 and stage 3. Removing the Doubler linearity from the equation (though not its gain, since that informs the gain required from the rest of the chain) allows for the contributions of the various configurations to be more easily distinguished. Plotting MER against the tilt allocation provides a useful way to consider two related dimensions of the problem at once.

5.3. Optimizing Gain and Tilt Placement

We were now able to investigate questions about optimal gain and tilt distribution in the LE. Consider Figure 8, which shows a variety of possible gain and tilt distributions, grouped into colors based on which of the first two stages has higher gain. . Two Doubler gain scenarios are considered. One scenario uses a Doubler gain of 21.5 dB and a second uses 28 dB gain. For each Doubler gain scenario we consider the effect of allocating the remaining required gain to the 1st and 2nd stages and use the tilt allocation between stages as the driving variable in the analysis.

The first and most apparent result is the observation that very high Doubler gain is ideal from a linearity perspective. A Doubler with 28 dB gain would enable the rest of the LE to be built with low gain stages without fear of non-linear contributions from the intermediate stage, even with low bias on that

component. With a 28 dB gain Doubler the remaining gain can be evenly split between 1st and 2nd stages, resulting in the blue plot in Figure 8.

Unfortunately, when designing within the legacy DC envelope for line extenders, process limitations constrain the gain to the low 20s. With a reasonable increase in bias voltage and current for the Doubler stage it would be possible to produce a 28 dB gain output stage with similar linearity to existing 12-14 W, 21.5 dB gain designs. That is generally outside the scope of this paper, but it bears consideration for situations where such a design change is possible.

Considering the scenario where the Doubler gain is 21.5 dB, the analysis shows best MER performance with the 2nd stage gain greater than the 1st stage. The various curves account for different levels of gain allocations between the 1st and 2nd stages. Regardless of the split it's favorable to have more gain in the 2nd stage with tilts evenly split between stages, resulting in MER into the Doubler above 53 dB. Placing too much gain in the 1st stage leads to distortion contributions from the 1st stage.

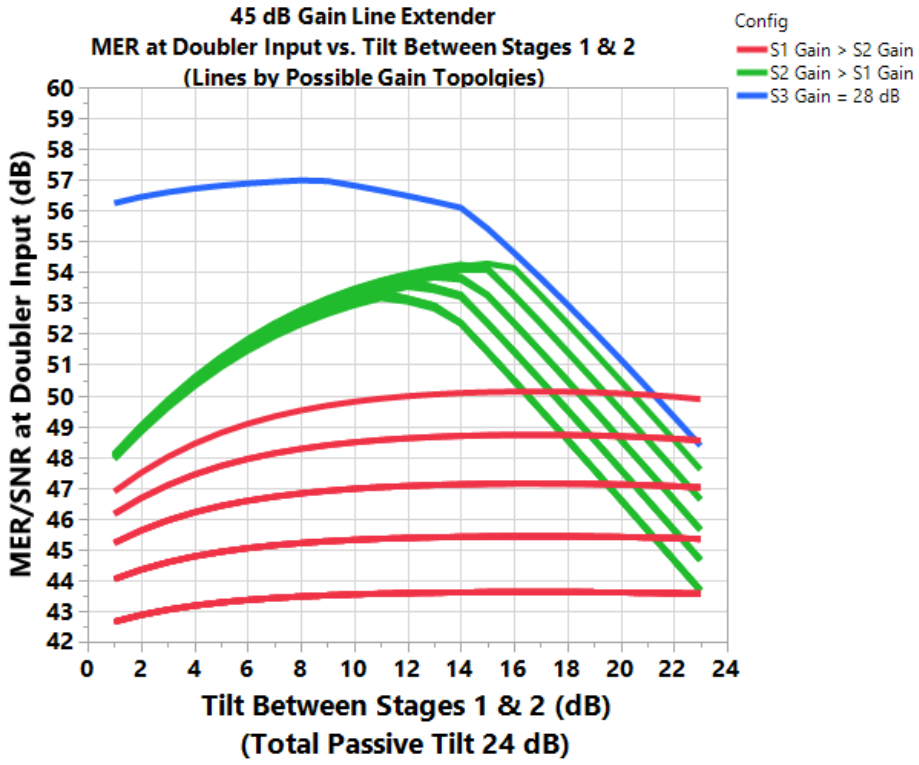

Figure 8 – Example Gain/Tilt Topologies

Starting from the known capabilities of the output Doubler, the ideal tilt split and gain of the first two stages can be solved simultaneously. Not surprisingly, given the number of factors which can contribute to degrading the SNR in the line extender, there is no simple set of linear equations which can be derived to produce the correct answer for all conditions. Further, such an answer would remain only a guideline as there are not enough varied active or passive elements available for actual design.

While a direct invocation of the simulation would be necessary to find the exact optimal topology for a given design target, there are two simplified approaches which both give reasonable approximations of optimum LE performance for LE gains in the range of 40-50 dB, given output TCP/tilt and passive loss criteria roughly similar to those outlined above. All gains are at 1.8 GHz:

1) Hold the gain of the second stage (~25 dB) and tilt split (~14/10) constant and allow stage 1 gain to vary
2) Hold the gain of the first stage constant (~19 dB) and allow stage 2 gain and tilt split to vary:

In general, the second approach proves to be more practical. It broadens the window for optimally splitting the tilt and for getting the correct gain. What this implies is that when the device gain varies due to temperature and the attenuator needs to be adjusted to compensate, the shift in performance as the arrangement of gain and tilt becomes "non-optimal" will be minimized. To demonstrate this, consider Figure 9 which shows an estimation of amplifier gain (and passive loss) shifting as a function of increasing or decreasing temperature, and the result of adjusting the attenuator to maintain 45 dB overall LE gain. The gains in this example are 19 dB for stage 1, 25 dB for stage 2, and 21.5 dB for stage 3.

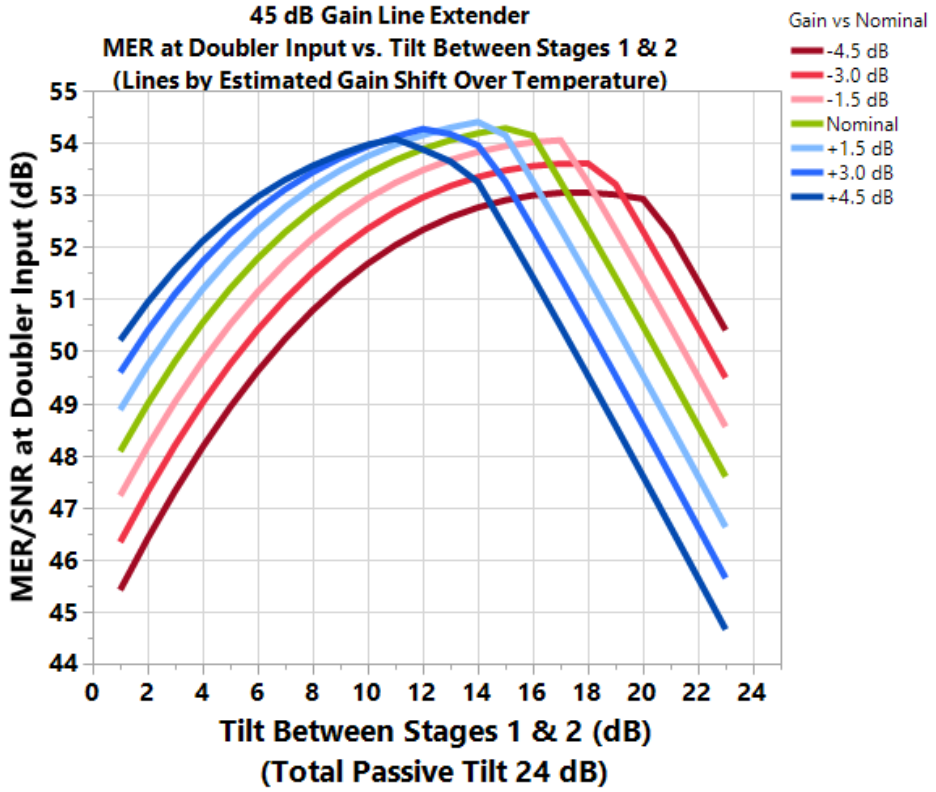

Figure 9 – Attenuator Compensating for Gain Shifts due to Thermals

5.4. Optimizing Bias Allocation

All the data so far presume some typical biasing for the components in question. Ideally, the overall DC budget for the downstream section of the LE will provide as much DC power as possible to the output Doubler while keeping the first two stages operating at just above the level where they would contribute meaningfully to the overall output SNR. To look at this, we'll consider the second method outlined previously, where stage 1 gain is held constant and stage 2 gain and tilt split are varied. Under these conditions, can any bias be borrowed for the Doubler?

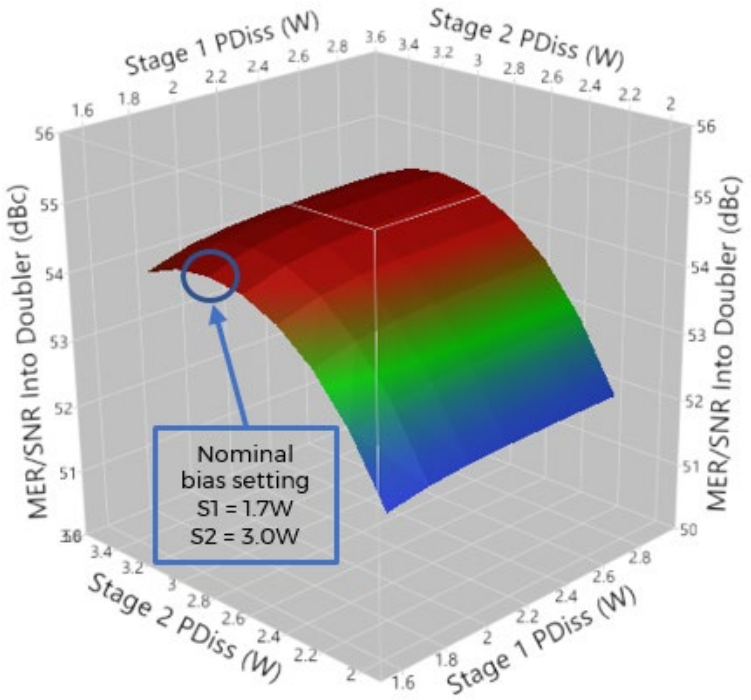

Figure 10 – SNR Into Doubler as a Function of Stage 1 and Stage 2 Power Dissipation

Simulation of optimal gain and tilt distribution for a 45 dB gain LE over stage 1 and stage 2 bias can be seen in Figure 10. With the modeled components, it would be possible to extract ~1 W from the second stage bias and transfer it to the Doubler, presuming that a change of incoming SNR to the Doubler from ~54 dB to ~52 dB would not negatively impact output performance. In our model, increasing the Doubler bias by 1 W was break even with the decreased incoming SNR to that stage, because the Doubler was already running at an optimized bias condition.

Optimizing the bias allocations within a given DC budget can be a sensitive process and would be best performed on prototype boards to directly observe the crossover point where improvement in Doubler linearity no longer overcomes degradation in earlier stage linearity.

It's worth noting that in theory, the bias and gain configurations could be simultaneously optimized to produce a slightly more favorable result. The devices were nominally biased well already, and the model would need to be significantly more precise throughout to benefit from such a small optimization.

5.5. Other Effects

There are a few other effects which can alter the model that are worth mentioning, the first of which is noise figure. The influence of noise figure for the input device is understood, and while it's relatively small, it grows larger as the overall LE gain increases or if too much tilt is placed after the first stage amplifier. For example, an optimally constructed 48 dB overall gain LE will see a ~0.5 dB change in MER coming into the Doubler for a 1 dB change in stage 1 noise figure. When considering a 42 dB gain LE, the change is only ~0.2 dB. More surprising is the fact that the second stage noise figure should also not be ignored. In this case the discrepancy between low and high gain LEs is more stark – at 42 dB overall gain, the effect of stage 2 NF is less than 0.05 dB, while at 48 dB overall gain, the effect is roughly 0.5 dB MER per 1 dB NF. This occurs because the optimal distribution of tilt and attenuation

pushes the input signal to the second stage as low as possible to avoid non-linearities behavior in that stage.

One last effect worth mentioning is that of the minimum insertion loss of the variable attenuator. We have made a very conservative assumption that this would be around 5 dB, but it is certainly possible with careful design to craft an attenuator with lower insertion loss (IL). In doing simulations with a minimum IL of 3 dB, we found that while it is overall a more favorable configuration, it does not provide as much benefit as one might expect. Less attenuation required between the first two stages allows for more tilt to be placed before the second stage and enables the use of a lower gain input stage (or a lower gain second stage, although this approach is less beneficial per our analysis). Excepting some fringe cases, we found that the overall MER improvement into the Doubler from a 2 dB change in attenuator minimum loss was on average about 1 dB. A lower IL for the attenuator does enable more design flexibility, provided it remains well-behaved through its full attenuation range and is useful for incrementally improving linearity.

5.6. Simulation Summary

In the end, it's impossible to provide hard and fast rules for overcoming all the challenges that designing a line extender entails. However, some guidelines have been provided for managing the interrelated set of variables that must be considered. We hope that these will prove useful in the design of line extenders for 1.8 GHz going forward. The simulations helped us identify the concept of developing a family of interchangeable downstream amplifier components.

5.7. Resulting LE Performance

Using the measurement-based models we considered overall cascaded performance as a function of the tilt spilt using the previously described parameters. The results are shown in Figure 11. Variable attenuation is placed between stage 1 and stage 2. Gains for stage 1, stage 2, and stage 3 are 19.0 dB, 25.0 dB, and 21.5 dB respectively. Coaxial port output TCP is set to 70.0 dBmV and downstream consumption in amplifier components is limited to 18.5 W. Upstream amplifier component prototypes capable of 40 dB gain and 69 dBmV TCP from 108 MHz through 684 MHz consumed 3.5 W. This brings the combined DC consumption to 22 W. The results show relatively consistent MER performance > 45 dB with the best option being an even splitting of the passive tilt.

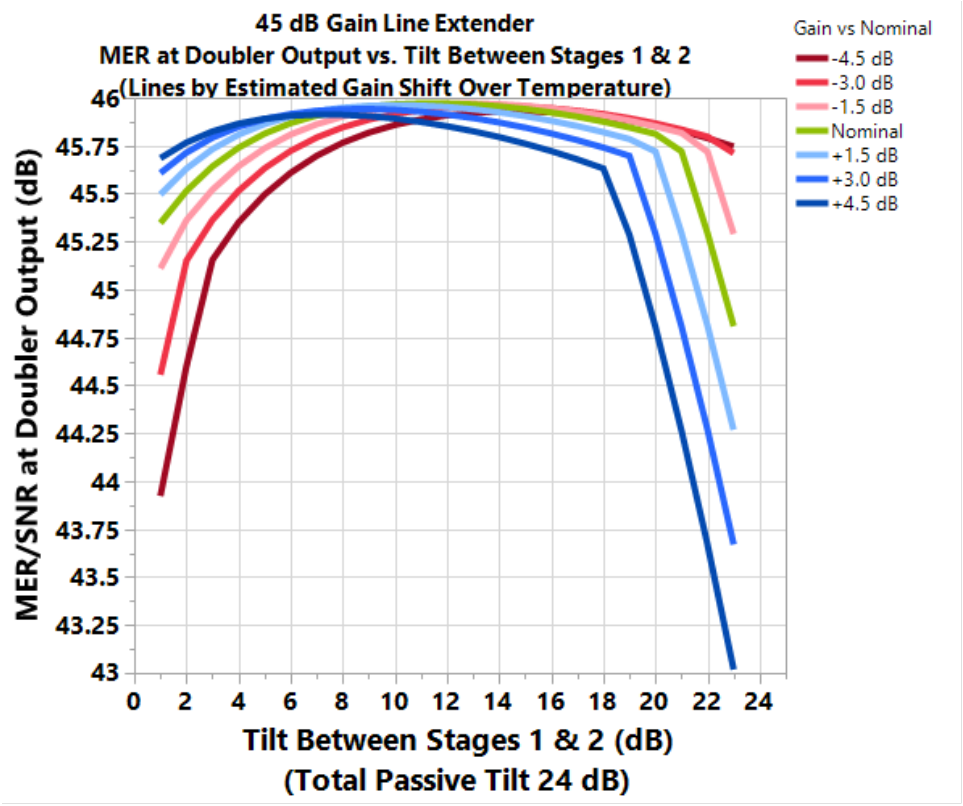

Figure 11 – Modeled MER Performance of 45 dB Line Extender

5.8. Higher Output Levels

Although the focus has been on staying within the existing LE power budget, it is feasible to increase the Tx TCP from the Doubler by adjusting the design and biasing scheme. Prototype Doublers have shown ability to output > 77 dBmV TCP but require near the maximum SOT115 power dissipation of 18 Watts. Getting higher output levels would best be approached with a new packaging design for better thermal and RF characteristics.

6. Noise Considerations

6.1. Downstream Point of Entry

Thus far we have focused on optimum design for maximizing LE Tx power and MER performance within legacy boundary conditions. The recent DOCSIS 4.0 specification establishes an input power range of +15 to -30 dBmV per 6 MHz channel. Low input levels are likely for distant reaches in a coaxial plant due to a combination of lower-grade coaxial cable, unfavorable tap location, and long drop length. In these cases, the overall SNR performance will be dominated by the Rx sensitivity and not distribution plant MER contributions.

To address the situation, we designed a low noise amplifier (LNA) stage with an integrated low loss linear bypass switch suitable to handle the wide input dynamic range. The bypass mode can be activated about midway within the range thereby alleviating the need for the LNA to have excellent linearity over the full range of input powers.

We used a linear pHEMT process with good noise characteristics. The process is consistent with a low-cost high-volume environment, not unlike mobile device applications where higher performance GaAs processes provide favorable cost-benefit to the network.

Simulated noise figure for the LNA path was <1.7 dB with a forward gain of 17 dB. Considering a secondary gain stage with noise figure of 5.0 dB, the overall noise figure can be < 2.0 dB. Comparing to today's cascaded noise figure of 4.5 dB, it's possible to improve the SNR performance, and hence the achievable data rate, for some locations at extreme locations in the plant. Just as in the case of maximizing Tx performance for added link budget with careful design, improving receiver sensitivity provides similar opportunity. Although improvement in distribution plant MER provides benefit across the serving area, input noise figure improvements at the point of entry are particularly helpful at extreme network locations. Improved receiver sensitivity is available to help overcome the significant link budget implied with Extended Spectrum deployments over lossy legacy infrastructure.

6.2. Upstream

PHEMT devices feature high intrinsic transconductance and excellent bandwidth. However, compared to other process technologies they unfortunately have poor 1/f noise characteristics. Often, 1/f noise corners for pHEMT devices can be around 30 MHz The 1/f noise corner depends on semiconductor start material properties which are generally not well controlled by epi vendors and fabricators alike who commonly target much higher volumes not sensitive to 1/f considerations. For these reasons pHEMT devices make inconsistent input stage devices in upstream applications. They may make suitable output sections for upstream applications since noise performance is dominated by input stage contributors. On the other hand, bipolar devices have 1/f noise corners well below 100 KHz and are better choices for input stages in upstream amplifiers.

7. Conclusion

Migrating to an extended spectrum architecture will require careful network planning and design of network elements. Given the magnitude of overcoming the substantial increase in passive losses we sought to design a family of components that could best serve the industry in this task. As with past upgrade cycles, newer component technology is available to help facilitate an upgrade with minimal disruption to existing networks. These technologies are best utilized by opening the design window to optimally allocate gain, bias, attenuation, and tilt in ES equipment design.

Abbreviations

AGC	automatic gain control
BOM	bill of materials
C	Centigrade
dB	decibel
dBmV	decibel relative to 1 millivolt
DC	direct current
DOCSIS	Data-Over-Cable Service Interface Specifications
DPD	digital pre-distortion
ES	extended spectrum
GaAs	gallium arsenide
GHz	gigahertz
HFC	hybrid fiber coax
IL	insertion loss
kHz	kilohertz
LE	line extender
LNA	low noise amplifier
LPDC	low density parity check
MER	modulation error ratio
MHz	megahertz
NF	noise figure
NMS	network management system
OFDM	orthogonal frequency-division multiplexing
QAM	quadrature amplitude modulation
QFN	quad-flat no leads
pHEMT	pseudomorphic high-electron-mobility transistor
PoE	point of entry
RF	radio frequency
Rx	receive
SCTE	Society of Cable Telecommunications Engineers
SNR	signal-to-noise ratio
TCP	total composite power
Tx	transmit
V	volt
W	watt

Bibliography & References

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