SCTE·ISBE CABLE-TEC EXPO 2018 | ATLANTA, GA OCTOBER 22-25

2018 Fall Technical Forum SCTE·ISBE • NCTA • CABLELABS

Delta-Sigma Modulation for Next Generation Fronthaul Interface

A Technical Paper prepared for SCTE•ISBE by

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Introduction

The emerging video-intensive and bandwidth-consuming services, e.g., virtual reality, augmented reality, immersive applications, are driving the explosive growth of mobile data traffic [1-3], making radio access networks (RAN) the bottleneck of user experience.

1. Challenges to C-RAN and CPRI

During the 4G era, to enhance the capacity, coverage, and flexibility of mobile data networks, centralized/cloud-RAN (C-RAN) was proposed [4] to separate the baseband processing functions from base stations (BS) at cell sites, and consolidate them into a centralized baseband unit (BBU) pool, which not only simplifies each BS to a remote radio head (RRH), but also enables the radio coordination among multiple cells [5-8]. In this way, C-RAN architecture is divided into two segments, i.e., backhaul from 4G evolved packet core (EPC) to BBUs and fronthaul from BBUs to RRHs, and common public radio interface (CPRI) proposed by the CPRI cooperation, including Ericsson, Huawei, Nokia, and NEC, was adopted as the fronthaul interface [9].

However, it was quickly realized that, CPRI, as a digitization interface developed for narrowband radio access technologies (RATs), e.g., UMTS (CPRI version 1 and 2), WiMAX (v3), LTE (v4), and GSM (v5) [9], suffers from limited scalability due to its low spectral efficiency and requires tremendous data traffic in the fronthaul network segment. Moreover, CPRI features constant fronthaul data rate, which is independent to the actual mobile traffic, but scales with the antenna number, and therefore, cannot support statistical multiplexing of multiple traffic flows. All these features make CPRI the bottleneck of C-RAN, especially for the massive MIMO and large-scale carrier aggregation applications.

To circumvent the CPRI bottleneck, three strategies were developed, including the analog fronthaul, CPRI compression, and new function splits or next generation fronthaul interface (NGFI). The analog fronthaul technique transmits mobile signals in their analog waveforms using radio-over-fiber (RoF) links [10, 11]. It features high spectral efficiency, simple, low-cost system implementations, but is susceptible to nonlinear and noise impairments [12-14]. The CPRI compression solutions rely on the existing CPRI interface but manage to reduce the fronthaul data rate via compression algorithms [15-17] or nonlinear quantization techniques [18-20]. It requires additional hardware complexity and cost on both sides of BBU and RRH.

By rethinking the RAN architecture and reorganizing its function distribution [21], the next generation RAN (NG-RAN) architecture is proposed with new function split options other than CPRI [22-24]. These new function split options include option 6 and 7 proposed by the 3rd Generation Partnership Project (3GPP) telecommunications standard [25-27], and Ethernet CPRI (eCPRI) specification proposed by the CPRI cooperation [28, 29].

2. Motivation

Both CPRI compression and new function split solutions require a complete RF layer implemented in the analog domain at each remote cell site, which inevitably increases the hardware complexity and cost of each small cell and hinder the wide deployment of small cells in the 5G era. Different from the option 6, 7 or eCPRI, which moves the split point away from the PHY-RF layer interface to a higher level, we propose a new split option9, which lowers the split point into the RF layer. Compared with CPRI, it saves fronthaul data traffic by 50-75%; compared with other new function split options, such as 6, 7, eCPRI, it maintains the centralized architecture and significantly reduce the cost and complexity of remote cell sites, and thus facilitates small cell deployment in the 5G era.

The proposed option 9 function split implements all-digital RF transceiver by exploiting delta-sigma modulation, where the RF layer is split into high-RF layer centralized in the central unit and low-RF layer distributed in the remote cell site. It not only improves the spectral efficiency compared with CPRI, but also eliminates the need of analog RF devices, such as digital-to-analog converter (DAC), local oscillator (LO) and mixer at the remote cell site, making simple, low-cost, and energy-efficient small cell possible.

Meanwhile, the vision of software defined radio (SDR) is to push the AD/DA conversion as close as possible to the antenna, so that both baseband and RF processing are carried out into the digital domain for enhanced flexibility and compatibility to multiple radio access technologies (multi-RATs) with different PHY layer specifications. SDR also enables dynamic reconfiguration of function split, since 5G scenarios can have drastically different requirements in terms of data rate and latency, e.g., enhanced mobile broadband (eMBB), ultra-reliable low latency communication (uRLLC), and massive machine type communication (mMTC), which can significantly benefit from reconfigurable function split.

3. State-of-the-Art

As a cornerstone of SDR, all-digital RF transceiver based on delta-sigma modulation has attracted intensive research interest due to its low cost and flexibility to accommodate multi-RAT operations. Both transmitter [30-52] and receiver [53-59] designs have been reported, and various delta-sigma modulators, including lowpass [30, 32-34, 36-39, 41-45, 47, 48], bandpass [31, 35], and multiband [40, 49-52] designs have been demonstrated using either FPGA or CMOS. A state-of-the-art of delta-sigma modulation is presented in the appendix. In this work, we present a fourth-order bandpass delta-sigma modulator, which has the highest sampling rate and widest reported signal bandwidth for fourth-order modulation.

In [60, 61], we first proposed to use delta-sigma modulation to replace CPRI to improve the spectral efficiency of fronthaul, and successfully improve the fronthaul spectral efficiency by four times. In [62, 63], we first proposed that delta-sigma modulation can be used for N+0 fiber deep migration and transmitted 20 data over cable service interface specification (DOCSIS) 3.1 channels using delta-sigma modulation via a single-wavelength 128 Gb/s coherent optics link. All the modulators in these early works, however, were realized by offline processing, and so far, there is no real-time demonstration of delta-sigma modulation for NGFI application.

In this paper, we propose a new function split option 9 for NGFI enabled by delta-sigma modulation, and for the first time, a real-time FPGA-based delta-sigma modulator is demonstrated. The proposed option 9 split not only improves the fronthaul spectral efficiency, but also simplifies the small cell design and reduce the cost of small cell deployment in dense urban areas. Furthermore, all-digital RF transceivers based on delta-sigma modulation enables SDR and mobile network virtualization, which enhances the compatibility of NG-RAN with multiple RATs, including 4G-LTE, Wi-Fi, and 5G-NR, etc.

NG-RAN and Function Split Options

1. Evolution of RAN

Figure 1 shows the evolution of RAN from 3G, 4G toward 5G. In the 3G era, both baseband and RF processing are carried out in the all-in-one BS, which is distributed at each cell site, as shown in Fig. 1(a). After RF processing, the mobile signals are fed to the antennas via coaxial cables due to the short distance between the BS and antenna. In the 4G era (Fig. 1b), C-RAN architecture was proposed to separate the baseband processing functions from the BS, and consolidates them into a centralized BBU pool, so each

BS is simplified to a RRH. Since the fiber distance between the BBU and the RRH is extended to tens of kilometers, mobile signals are transmitted over digital fiber links via CPRI interface.

In the 5G era (Fig.1c), to address the CPRI bottleneck, NG-RAN architecture is proposed with additional function split, with the baseband functions originally from the BBUs of C-RAN are now distributed into the central units (CU) and distributed units (DU). The NG-RAN architecture is thus divided into three segments, i.e., backhaul from the mobile edge computing (MEC) to CU, midhaul from the CU to the DU, and fronthaul (NGFI) from the DU to the remote radio unit (RRU), and there are two function split interfaces, high layer split (HLS) between the CU and the DU, and low layer split (LLS) between the DU and the RRU. For the HLS, option 2 has been adopted by 3GPP as a standard; whereas for the LLS, there is still debate among several different candidates, including option 6, 7 proposed by 3GPP, and eCPRI specification proposed by CPRI cooperation.

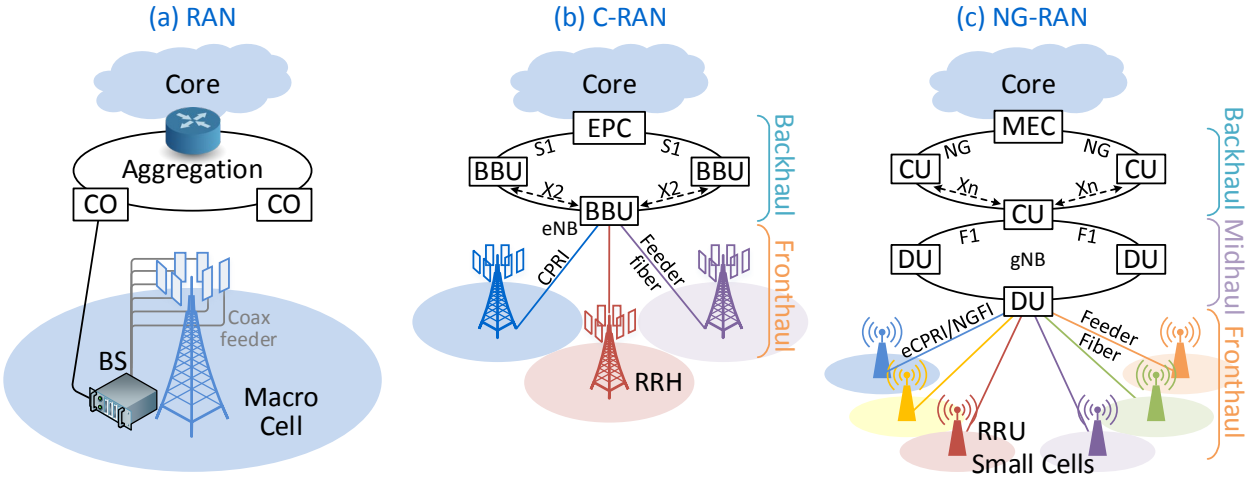

Figure 1 - Evolution of radio access network (RAN). (a) 3G RAN. (b) 4G cloud/centralized-RAN (C-RAN). (c) 5G next generation-RAN (NG-RAN).

2. Function Split Options

Figure 2 shows a comprehensive summary of function split options. Fig. 2(a) presents the block diagram of functions in different layers, including radio resource control (RRC), packet data convergence protocol (PDCP), radio link control (RLC), media access control (MAC), physical (PHY), and RF layers [23-26]. Function split options proposed by 3GPP are labeled in black, and options from eCPRI specification are labeled in blue. For the HLS, option 2 between the PDCP and RLC layers has been adopted by 3GPP as a standard; whereas for the LLS, there is still debate among several candidates, including option 6 (MAC-PHY), option 7 (high-low PHY), and eCPRI.

Fig. 2(b) shows the C-RAN architecture with option 8 (CPRI) split between the BBU and the RRH. Fig. 2(c) and (d) show the NG-RAN architectures with option 2 as the HLS between the CU and DU, and option 6 (MAC-PHY) or 7 (high-low PHY) as the LLS between the DU and the RRU. Fig. 2(e) shows LLS of option 9, where the high-RF layer is implemented in the digital domain and centralized in the DU, leaving only the low-RF layer in the RRU. In Figure 2, it should be noted that all existing LLS options, including 6, 7, 8, as well as eCPRI, all require a complete RF layer implemented in the analog domain at each remote cell site, including DAC, LO, mixer, power amplifier (PA), and bandpass filter (BPF), which increases the system complexity and cost of small cells.

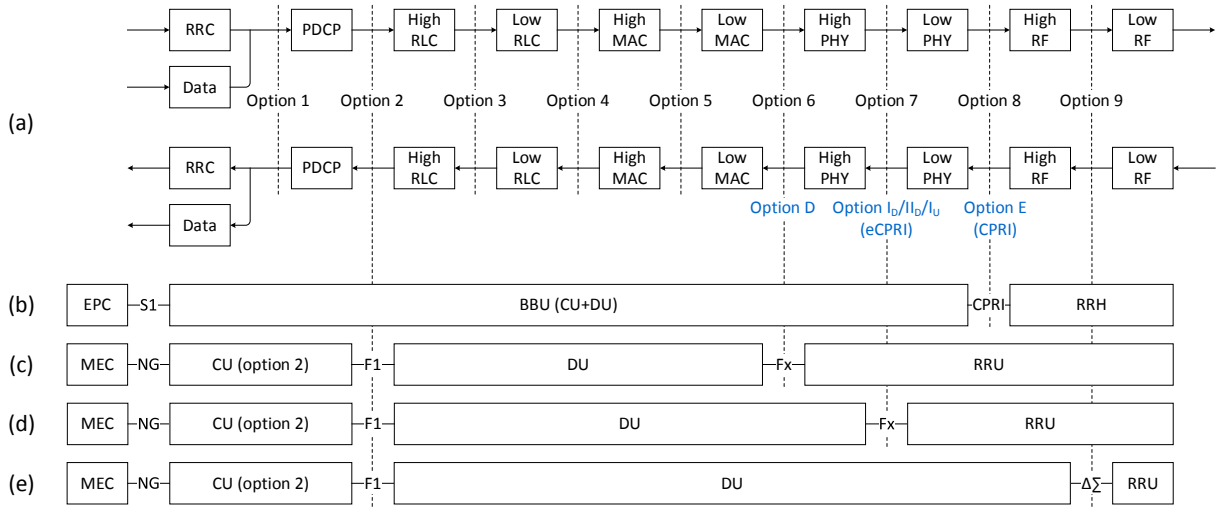

Figure 2 - Function split options. (a) A complete list. (b) C-RAN with option 8 (CPRI) split. (b-d) NG-RAN with option 2 as HLS, and option 6 (MAC-PHY), 7 (high-low PHY), and 9 (high-low RF) as LLS.

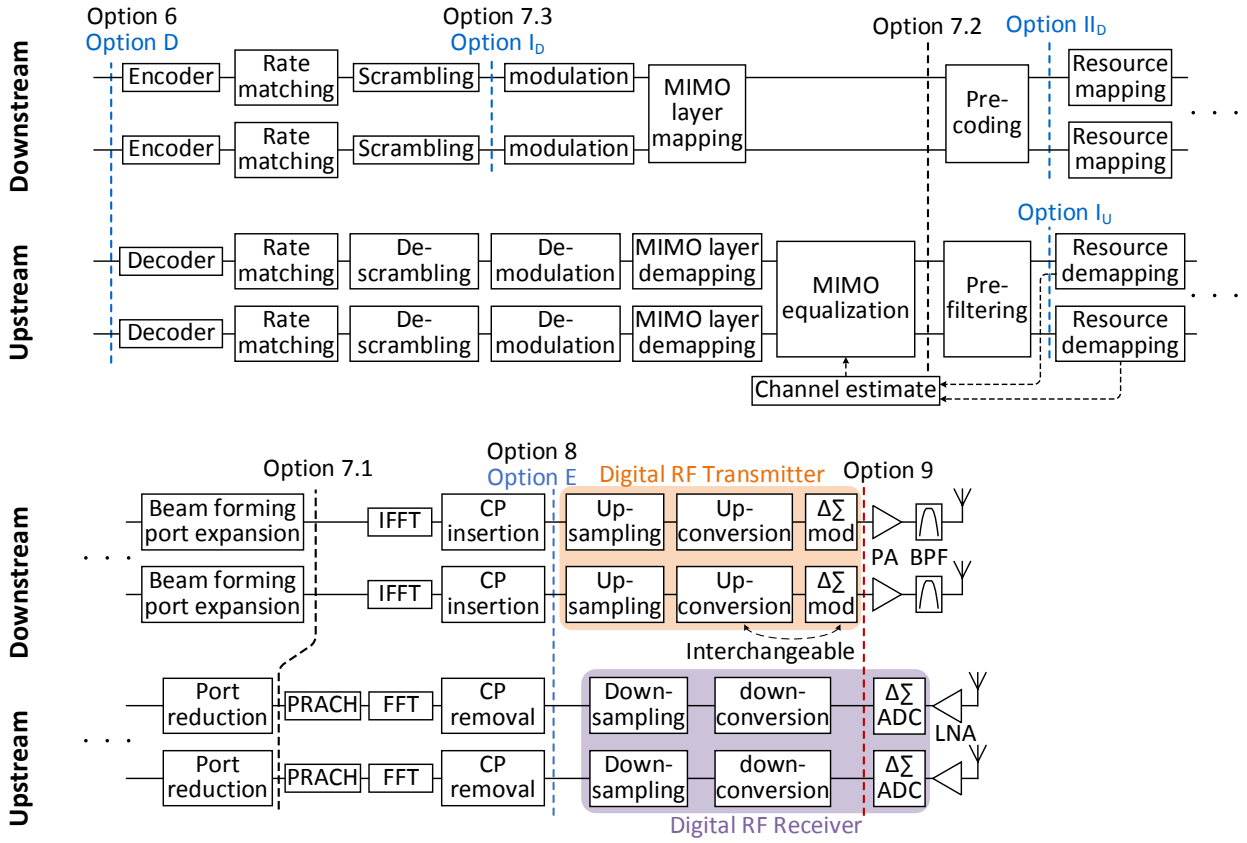

Figure 3 - Detailed function block diagram of the PHY and RF layers.

Figure 3 shows a detailed block diagram of functions in the PHY and RF layers. Function split options proposed by 3GPP are labeled in black, and options from the eCPRI specification are labeled in blue. The MAC-PHY split is defined as option 6 by 3GPP or option D in eCPRI specification; PHY-RF split is defined

as option 8 by 3GPP or option E in eCPRI specification. Within the PHY layer, both 3GPP and CPRI cooperation define three different options, 7.1, 7.2, 7.3, and I_D, II_D, I_U, respectively. Only 7.1 and 7.2 are bi-directional; all the rest are for one direction only. 7.3, I_D, II_D are for downstream, and I_U for upstream.

In this paper, we propose a new function split option 9, which lowers the split point into the RF layer. Compared with CPRI, it saves fronthaul data traffic by 50-75%; compared with other new function split options, such as 6, 7, eCPRI, it maintains the centralized architecture and significantly reduce the cost and complexity of remote cell sites, and thus facilitates small cell deployment in the 5G era.

In the RF layer of Figure 3, for downstream, an all-digital RF transmitter is used based on a bandpass delta-sigma modulator, and option 9 split takes place after the bandpass modulator, which encodes the discrete-time multibit signal into a one-bit data stream and transmits it from the DU to the RRU via digital fiber links. For upstream, a digital RF receiver based on a continuous-time delta-sigma ADC is used to digitize the received analog signal to discrete levels, and option 9 split takes place after the delta-sigma ADC, transmitting digital bits representing these discrete levels from the RRU back to the DU. With the help of delta-sigma modulation/ADC, the RF layer is implemented in the digital domain.

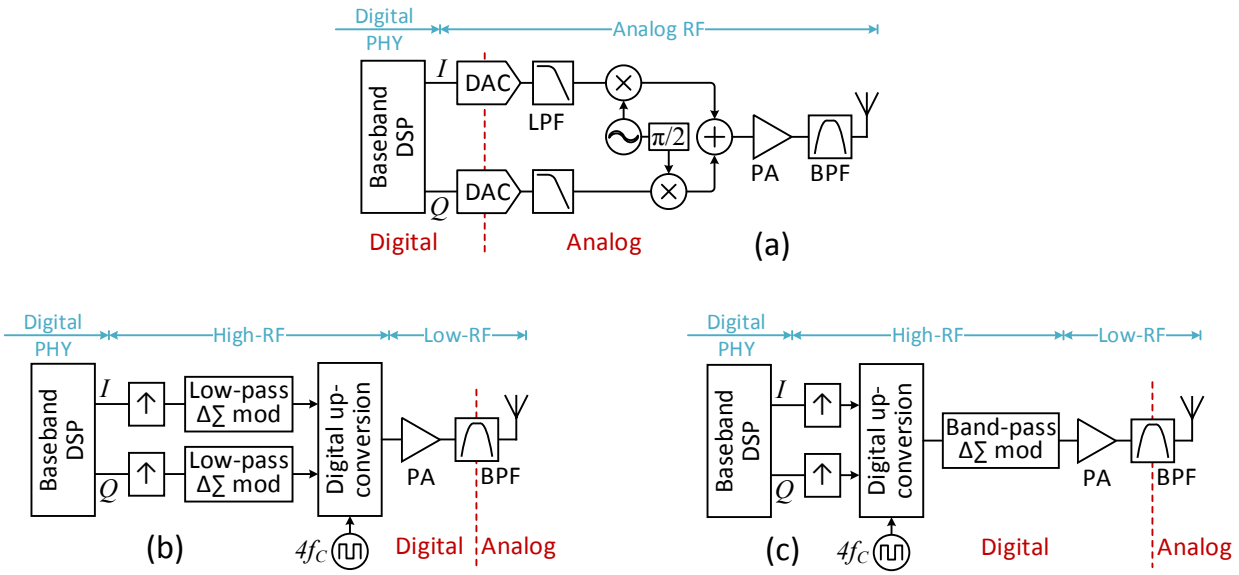

Figure 4 - Architectures of analog RF transmitter (a) and digital RF transmitters (b, c).

The architectures of digital RF transmitter are presented in Figure 4. Except for option 9, all other LLS options, including 6, 7, 8, and eCPRI, implement the RF layer in the analog domain, and require a complete RF layer at each remote cell site, which inevitably increases the system cost and complexity of each small cell. Fig. 4(a) shows an analog RF transmitter, which consists of DAC, LO, mixer, BPF, and linear PA. The DAC separates the digital processing of baseband signals from the analog processing of RF signals.

For option 9 split, on the other hand, the RF layer is implemented in the digital domain, and there is no need of analog LO, mixer, or linear PA. Fig. 4(b) and (c) shows the architectures of digital RF transmitter based on lowpass or bandpass delta-sigma modulators. In Fig. 4(b), baseband I and Q signals are first up-sampled, then encoded by two low-pass delta-sigma modulators, respectively, where the multibit baseband I/Q samples are converted to two one-bit data streams. A digital frequency up-converter then combines the I/Q bit streams and converts them to a radio frequency. The up-converted bit stream is transmitted from DU to RRU for wireless emission. In Fig. 4(c), the I and Q samples are first up-converted to a radio frequency, and then encoded by a bandpass delta-sigma modulator.

Since delta-sigma modulation utilizes noise shaping to push the quantization noise out of the signal band, in either case of Fig. 4(b) or (c), the analog mobile signal can be easily retrieved by a BPF at the RRU, which selects the desired mobile signal, while at the same time, retrieves its analog waveform by eliminating the out-of-band noise. Therefore, the conventional DAC used in Fig. 4(a) is now replaced by a simple low-cost BPF. This design also aligns with the view of digital RF transceiver to push the DAC as close as possible to the antenna, so both baseband and RF processing are carried out in the digital domain.

One advantage of all-digital RF transmitter is its flexibility and reconfigurability to different PHY layer specifications and carrier frequencies of multiple RATs. As a cornerstone to SDR, digital RF transceiver enables the virtualization of DU and RRU, making NG-RAN compatible with not only 5G-NR, but also 4G-LTE and Wi-Fi signals. Another advantage of all-digital RF transmitter is the signal fidelity. In Fig. 4(a), the analog RF signal is amplified by a PA with inevitable nonlinear impairments. But in Fig. 4(b, c), the BPF acts as a DAC, and the PA is placed before the BPF, which is still in the digital domain and dealing with digital bits. Therefore, switch-mode PAs can be used, which offers high power efficiency without nonlinear penalties. One limitation of digital RF transmitters is its high oversampling rate and high clock rate, which needs to be four times of the carrier frequency for digital up-conversion.

3. Comparison of Options 6, 7, 8, and 9

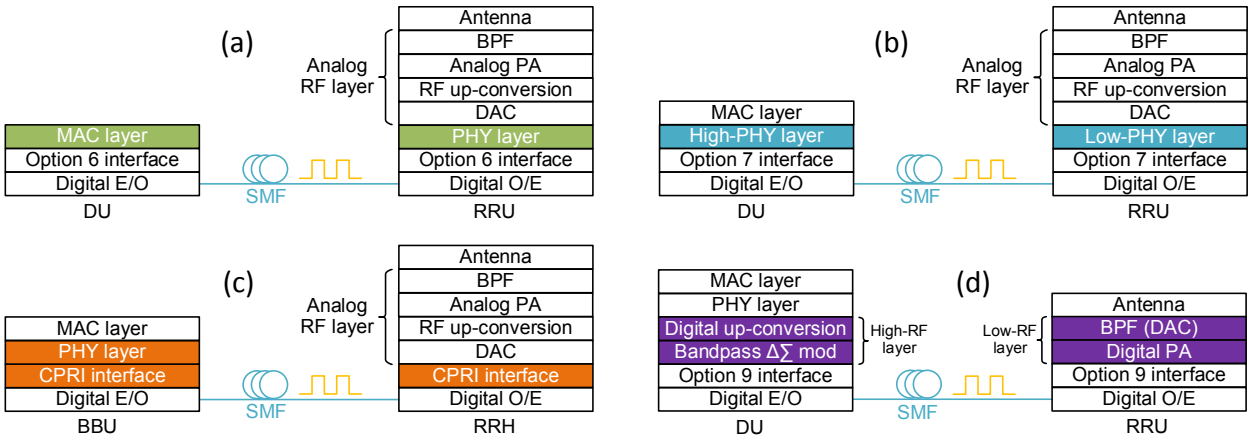

Figure 5 - Architecture comparison of different low layer split (LLS) options, including option 6 (a), 7 (b), 8 (c), analog fronthaul (d), and option 9 (e).

Figure 5 shows the architecture of different function split options, including 6, 7, 8, and 9. Fig. 5(a) shows the NGFI architecture with option 6 (MAC-PHY) split, where the MAC layer is centralized in DU, while both PHY and RF layers are distributed in the RRU. The baseband processing of the PHY layer is implemented in the digital domain; whereas the RF layer is implemented in the analog domain with DAC, LO, mixer, and PA. Since both PHY and RF layers are carried out at the RRUs, the complexity and cost of each cell site is high.

Fig. 5(b) shows the NGFI architecture with option 7 split. The high-PHY layer processing is carried out in the DU, and the rest low-PHY layer processing is implemented at the RRU. A complete RF layer is needed at each RRU, and it is implemented in the analog domain. Compared with CPRI, option 7 significantly reduces the fronthaul traffic, but also increases the cost and complexity of each cell site, which hinders the wide deployment of small cells.

Fig. 5(c) shows the fronthaul architecture with option 8 (CPRI) split, with the PHY layer centralized in the DU, and RF layer distributed at the RRUs. Like option 6 and 7, a complete analog RF layer is needed at

each RRU. CPRI has low spectral efficiency, requires tremendous fronthaul traffic, and has limited scalability for massive MIMO and carrier aggregation. Moreover, CPRI has a fixed chip rate (3.84 MHz), and can only accommodate UMTS (v1 and 2), WiMAX (v3), LTE (v4), and GSM (v5).

Fig. 5(d) shows the NGFI architecture with option 9 split, where both PHY and RF layers are implemented in the digital domain. PHY and high-RF layers, including digital up-conversion, delta-sigma modulation, are centralized in the DU; only low-RF layer functions, such as PA, BPF, antenna are left in the RRU. Since the BPF acts as an effective DAC, PA works in the digital domain, and switching-mode PA can be used with high power efficiency. Option 9 split enables a low-cost, DAC-free, and RF-simple design of RRUs, which significantly reduces the cost and complexity of cell site, and facilitates the wide deployment of small cells.

Since option 7 and 8 transmit digital baseband signals over NGFI, time division multiplexing (TDM) is needed to interleave the baseband I/Q components and components from different mobile signals. Time synchronization might be an issue considering the coexistence of legacy RAT and 5G-NR. On the other hand, option 9 transmits digital RF signal with I/Q components up-converted to the radio frequency, so frequency division multiplexing (FDM) can be used to accommodate multiband mobile signals.

Experimental Demonstration

1. Operation Principles of Delta-Sigma Modulation

Figure 6 and Figure 7 show the operation principles of Nyquist ADC and bandpass delta-sigma modulation, respectively. For a Nyquist ADC, each analog signal is digitized at baseband with a Nyquist sampling rate. The quantization noise is evenly distributed in the frequency domain. To reduce the quantization noise, multiple quantization bits are used for each sample, which leads to low spectral efficiency and large data rate after digitization and makes CPRI become the fronthaul bottleneck.

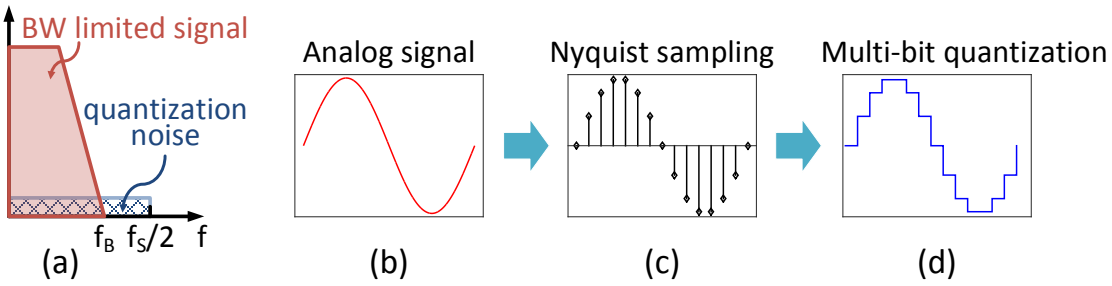

Figure 6 - Operation principles of Nyquist ADC. (a) Each signal is digitized at baseband. (b) Input analog signal. (c) Nyquist sampling. (d) Multi-bit quantization.

Different from Nyquist ADC, delta-sigma modulation trades quantization bit for sampling rate, using high sampling rate and only few quantization bits. After baseband processing, digital baseband signal is up-converted to radio frequency, then a bandpass delta-sigma modulation encodes the discrete-time multibit RF signal into a one-bit data stream. In Fig. 7(a), oversampling extends the Nyquist zone, so quantization noise can be spread over a wide frequency range. In Fig. 7(b), noise shaping technique pushes the quantization noise out of the signal band and separates the signal and noise in the frequency domain. After delta-sigma modulation, the signal waveform is transformed from analog to digital by adding out-of-band quantization noise. In Fig. 7(c), at RRU, a BPF filters out the desired signal, which not only eliminates the

out-of-band noise, but also retrieves the analog waveform as an effective DAC. Due to the noise shaping, the retrieved analog signal has an uneven noise floor.

In this paper, a one-bit bandpass delta-sigma modulator is implemented using a fourth-order cascaded resonator feedforward (CRFF) structure, shown in Fig. 7(d). There are four stages of feedback loops (z-1), each two cascaded together to form a resonator. There is a feedback path in each resonator, g_1, and g_2. The outputs of four stages are feedforwarded with coefficients of a_1, a_2, a_3, and a_4 to the combiner, then a one-bit quantizer acts as a comparator and outputs a one-bit (0/1) OOK signal.

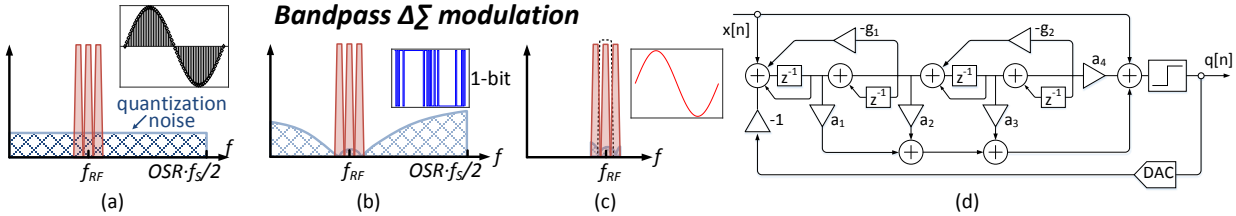

Figure 7 - Operation principles of bandpass delta-sigma modulation. (a) Oversampling. (b) Noise shaping. (c) BPF. (d) Cascaded-resonator feedforward structure.

2. Experimental Setup

Using the CRFF structure in Fig. 7(d), a real-time one-bit bandpass delta-sigma modulation is demonstrated with Xilinx Virtex-7 VX485T FPGA on a VC707 development board, shown in Fig. 8(a). A FPGA mezzanine card (FMC170) from 4DSP is inserted in the high-pin count (HPC) connector on VC707 as the input ADC. The FMC170 ADC has a sampling rate of 5 GSa/s and 10 quantization bits per sample. The input analog signal is first digitized to 10 bits, then fed to the FPGA to perform delta-sigma modulation, which transforms the 10 input bits to one output bit. After delta-sigma digitization, the output 5-Gb/s OOK signal is outputted via a multi-gigabit transceiver (MGT) port on VC707. The 5-GSa/s sampling rate of FMC170 is contributed by 32 time-interleaved ADCs, each working at 156.25 MSa/s, so the FMC170 clock rate is 156.25 MHz. In each clock cycle, it outputs 32 * 10 = 320 bits for 32 consecutive samples.

In Fig. 8(b), due to the speed limit of FPGA, a 32-pipeline architecture is designed to match the speed difference between the FPGA and FMC170. The input samples are de-serialized and sequentially filled into the first-in-first-out (FIFO) buffers in 32 pipelines. In each pipeline, once the input FIFO is filled up, delta-sigma modulation is performed, and the output bits are stored in an output FIFO. The output bits from 32 output FIFOs are serialized to a single bit stream. Since delta-sigma modulation is performed parallelly in all 32 pipelines, the operation speed of each line is relaxed to 156.25 MSa/s. Assuming each FIFO can store W samples with ΔW margin, since the input ADC has 10 bits per sample, each input FIFO has a size of $10(W+\Delta W)$ bits. The margin ΔW is allocated to each buffer for easy implementation. After delta-sigma modulation, the 10 input bits are transformed to one output bit, so the output FIFO has a size of $W+\Delta W$ bits.

Note that memoryless signal processing can be easily implemented by pipeline architecture, since the processing to each sample only depends on the current sample and has no relation with previous ones. After segmenting the input sample stream into several blocks, all blocks can be processed in parallel without performance penalty. On the other hand, delta-sigma modulation is a sequential operation with memory effect. The output bit not only depends on the current sample, but also previous ones, which makes it difficult to implement in a parallel way. There will be performance penalty to segment a continuous sample stream into several blocks, and the smaller block size is, the larger penalty will be. By making a tradeoff between performance penalty and the memory usage on FPGA, we choose a buffer size of W = 20k with

margin of ΔW = 2K. There have been several parallel processing techniques reported for high-speed, wide bandwidth delta-sigma modulators, including polyphase decomposition [44, 45], look-ahead time-interleaving [47, 48]. For a proof-of-concept experiment, here we only demonstrate the basic idea of pipeline processing with large buffer size. With the help of these parallel processing techniques, buffer size and processing latency can be significantly reduced.

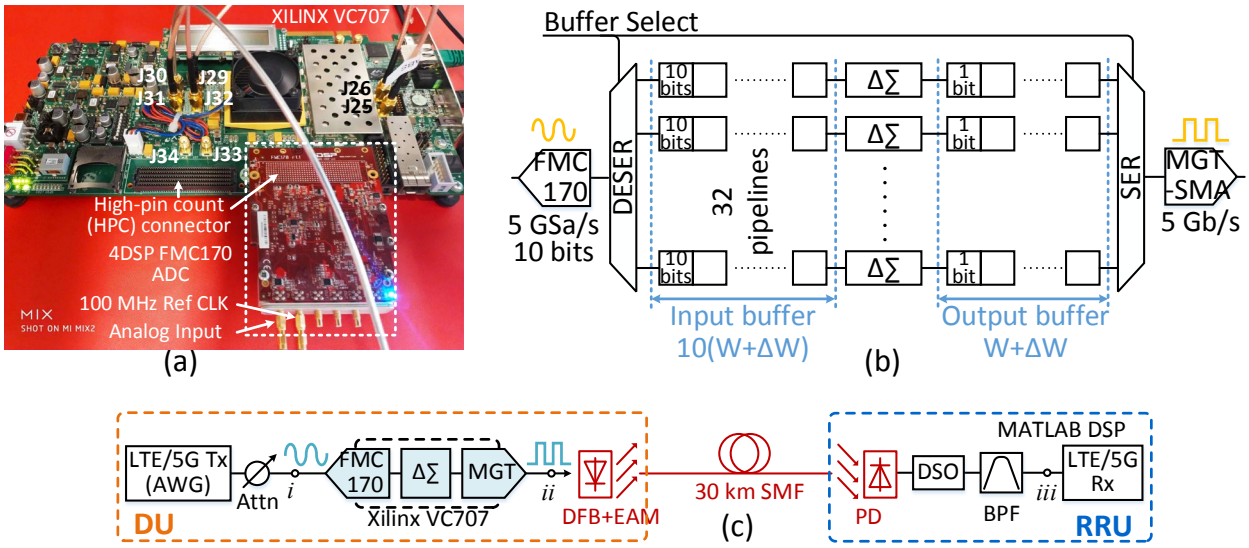

Figure 8 - Experimental setup. (a) Xilinx Virtex-7 VX485T FPGA on VC707 development board with 4DSP FMC170 ADC. (b) 32-Pipeline architecture. (c) Optical testbed.

Fig. 8(c) shows the experimental testbed. Carrier aggregated LTE/5G signals are generated by a Tektronix 7122C arbitrary Waveform Generator (AWG), then captured by the FMC170 ADC working at 5 GSa/s. The FPGA works as a one-bit bandpass delta-sigma modulator, transforming the 10 input bits to one output bit, and outputs a 5-Gb/s OOK signal. The OOK signal is delivered from DU to RRU via a digital fiber link, consisting of a 12.5 Gb/s Cyoptics DFB+EAM, 30-km single-mode fiber, and a 10 Gb/s Discovery optical receiver. 5-Gb/s error free transmission is achieved and the received OOK signal is captured by a 20 GSa/s Keysight data storage oscilloscope (DSO) MSOS804A and followed by real-time MATLAB DSP for bandpass filtering and LTE/5G receiving.

Four experimental cases are designed to verify the proposed all-digital transmitter based on delta-sigma modulation, and their OFDM parameters are listed in Table 1. 30 kHz subcarrier spacing is used for 5G signals with FFT size of 4096 and 122.88 MSa/s sampling rate. The number of active subcarriers is 3300, and the signal bandwidth of each 5G carrier is 99 MHz. The system performance is evaluated by the error vector magnitude (EVM) of received signals, and 3GPP requirements of different modulations are listed in Table 2 [64]. Note that the EVM requirement of 1024-QAM is first specified by TS36.104 V15.2.0 in 03/2018. Since this work was done earlier than that date, we use a stricter criterion of EVM < 2%.

Table 1 - OFDM parameters of 4G-LTE and 5G-NR Signals Used in the Experiments

Case	Signals	Sampling rate (MSa/s)	FFT size	Subcarrier spacing (kHz)	Data subcarriers	Carrier number	Actual BW (MHz)	Modulation (QAM)
I	5G-NR	122.88	4096	30	3300	1	99	1024
II						2	198	256*2
III	4G-LTE	30.72	2048	15	1200	10	180	256*6, 1024*4
IV						14	252	1024*2, 256*4, 64*8

Table 2 - EVM Requirements from 3GPP TS 36.104 V15.2.0 [64]

Modulation	QPSK	16-QAM	64-QAM	256-QAM	1024-QAM
EVM (%)	17.5	12.5	8	3.5	2.5 (2)*

* The EVM requirement of 1024-QAM was first specified by TS 36.104 V15.2.0 in 03/2018. Since this work is done before that date, we used a stricter criterion of 2%.

In Case I, one 5G carrier with 1024-QAM and 99-MHz bandwidth is used, and the EVM performance of received signal is less than 1.25%. In case II, two 5G carriers with 256-QAM are used. Since the signal bandwidth is doubled to 198 MHz, the oversampling rate (OSR) is halved with reduced signal-to-noise ratio (SNR). So lower modulation format is used to accommodate the increased EVM, and less than 2.83% EVM is achieved for both 5G carriers. Case III and IV deal with LTE signals. In Case III, 10 LTE carriers are used with different modulations loaded on different carriers, depending on their SNR. As shown in Table 1, there are four carriers with sufficient SNR to support 1024-QAM, whereas the rest six carriers supporting 256-QAM. Similarly, in the 14 carriers in Case IV, there are two 1024-QAM, four 256-QAM, and eight 64-QAM. The reduction of modulation formats is due to the wider signal bandwidth and increased quantization noise.

3. Experimental Results

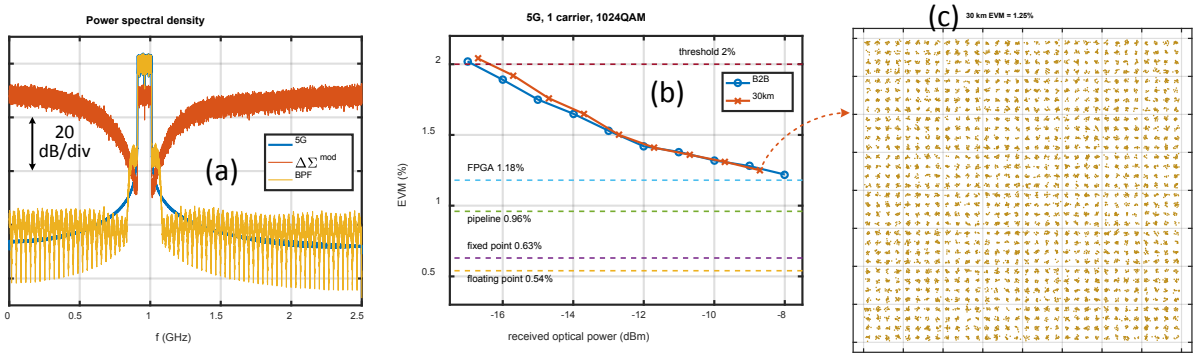

Figure 9 - Experimental results of Case I. (a) Electrical spectra of input analog signal, OOK signal after delta-sigma modulation, and retrieved analog signal after BPF. (b) EVM vs received optical power. (c) Received constellation after 30-km fiber.

The experimental results of Case I are shown in Figure 9. One 5G carrier with 1024-QAM and 99 MHz bandwidth centered at 960 MHz is generated by the AWG and converted to a 5-Gb/s OOK signal by the bandpass delta-sigma modulator on FPGA. Fig. 9(a) shows the RF spectra of input and output signals of the delta-sigma modulator. The input 5G signal at point i in the experimental setup (Fig. 8c) is labeled in blue; OOK signal after FPGA at point ii in red; the retrieved analog signal after BPF at point iii in yellow. For the retrieved analog signal, the adjacent channel leakage ratio (ACLR) is determined by the residual out-of-band noise after BPF. For easy implementation, a finite impulse response (FIR) Kaiser window filter with 40 dB out-of-band antennation was used. By using a filter with higher out-of-band antennation, it is not difficult to achieve the 44.2 dB ACLR requirement specified in 3GPP TS 36.141 [65]. Fig. 9(b) shows the EVM of the retrieved 5G signal as a function of the received optical power. Verilog simulation results, including floating point, fixed point, and pipeline, are also presented to show the step-by-step FPGA implementation and the performance penalty in each step. Compared with back-to-back transmission, there is no EVM penalty observed after 30-km fiber, and the received constellation is shown in Fig. 9(c).

The experimental results of Case II are shown in Figure 10. Two 5G carriers with 198-MHz total bandwidth and 256-QAM are converted to a OOK signal by the bandpass delta-sigma modulator on FPGA. Compared

with Case I, lower modulation formats are employed due to the doubled signal bandwidth and increased quantization noise. The electrical spectra of the input analog signal (point i in Fig. 8c), OOK signal (point ii), and retrieved analog signal (point iii) are presented in Fig. 10(a). EVMs of both carriers as functions of received optical power are shown in Fig. 10(b). After 30-km fiber transmission, EVMs of both carriers are less than 2.80% and 2.83%, satisfying the 3.5% requirements of 3GPP. Constellations after 30-km fiber are shown in Fig. 10(c) and (d).

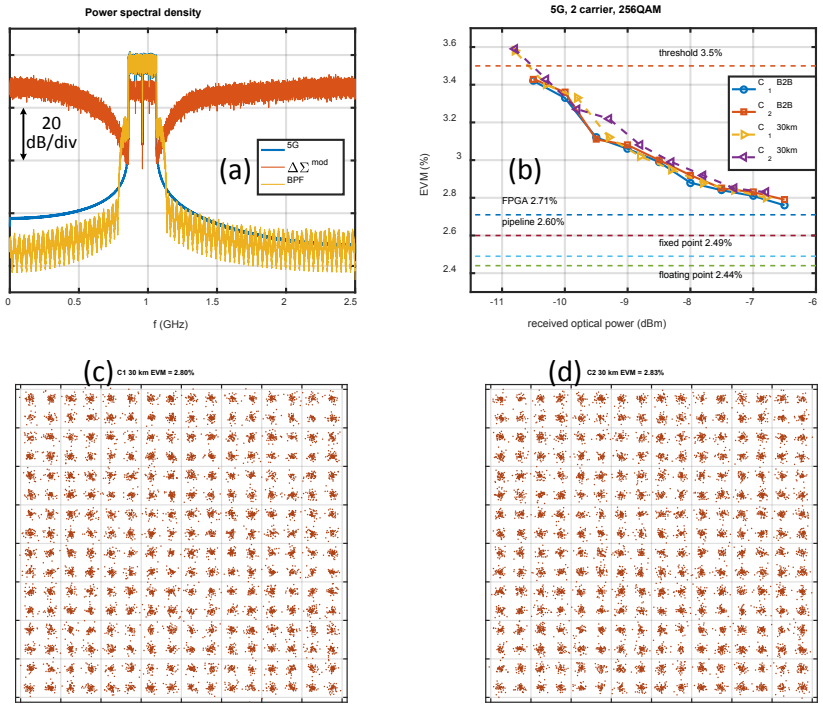

Figure 10 - Experimental results of Case II. (a) Electrical spectra of input analog signal, OOK signal after delta-sigma modulation, and retrieved analog signal after BPF. (b) EVMs vs received optical power. (c, d) Received constellations after 30-km fiber.

Figure 11 shows the experimental results of Case III, where 10 LTE carriers are used with different modulations assigned on different carriers according to 3GPP requirements. Fig. 11(a) shows the electrical spectra of input analog, OOK, and retrieved analog signals. Fig. 11(b) shows the EVMs of each LTE carrier. Within the 10 carriers, there are four carriers (2, 3, 8, 9) with EVM less than 2%, which can support modulation up to 1024-QAM; the rest six carriers (1, 4-7, 10) have EVMs less than 3.5%, and are able to support 256-QAM. The results of Case IV are shown in Figure 12. Due to the increased signal bandwidth, within the 14 carriers, there are only two carriers (3 and 12) with EVM smaller than 2%, and they can support modulation of 1024-QAM. There are four carriers (2, 4, 11, 13) with EVM less than 3.5% and used to carry 256-QAM; and the rest eight carriers (1, 5-10, 14) carry 64-QAM.

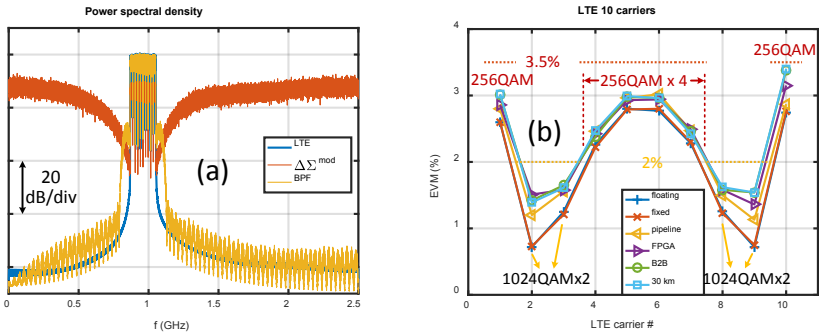

Figure 11 - Experimental results of Case III. (a) Electrical spectra of 10 LTE carriers. (b) EVMs of 10 LTE carriers.

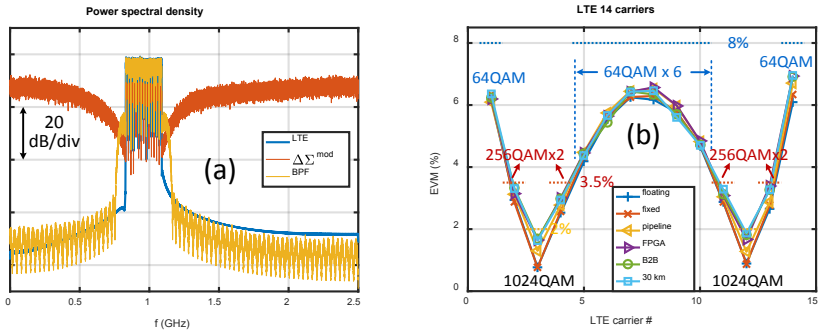

Figure 12 - Experimental results of Case IV. (a) Electrical spectra of 14 LTE carriers. (b) EVMs of 14 LTE carriers.

A summary of the resource utilization of Xilinx Virtect-7 FPGA is listed in Table 3. All four cases have similar resource usage, and the values listed are from Case II, 5G two-carrier aggregation. Note that 35.53% memory usage is due to the 22k buffer size in each pipeline. If time-interleaving technique is used, the memory usage can be significantly reduced.

Table 3 - Resource Utilization of Xilinx Virtex-7 VX485T FPGA

Resource	Utilization	Available	Utilization %
Logic cells	53362	485760	10.99%
DSP slices	64	2800	2.29%
Memory	13.18 Mb	37.08 Mb	35.53%
Transceivers	2	56	3.57%
I/O	181	700	25.86%
Max clock rate	156.25 MHz	650.20 MHz	N/A

4. Discussion

According to CPRI specification [9], a single 20-MHz LTE carrier requires 30.72 MSa/s * 15 bits/Sa * 2 = 921.6 Mb/s fronthaul capacity without considering control word and line coding (8b/10b or 64b/66b). So CPRI can take up to 9.22 Gb/s or 12.9 Gb/s to support 10 or 14 LTE carriers, respectively. In this work, all LTE carriers are encoded by a delta-sigma modulator and transmitted through a 5-Gb/s OOK link, which saves 45.8% or 61.2% data rate compared with CPRI.

Table 4 lists a comparison in terms of spectral efficiencies of CPRI, CPRI compression, and delta-sigma modulation. Since CPRI has one control word for every 15 data words of IQ samples [9] and uses line

coding of 8b/10b or 64b/66b, for a fair composition, no control word or line coding is considered in Table 4. Since CPRI-based solutions have smaller quantization noise and higher SNR than delta-sigma modulation, it will be fair to introduce two measuring metrics, bandwidth efficiency and bit efficiency. Bandwidth efficiency is defined as the ratio between the fronthaul data rate and LTE signal BW, measuring the required fronthaul capacity per unit of BW. Bit efficiency is the ratio between fronthaul data rate and the net information rate carried by LTE signals, measuring the mapping efficiency from fronthaul traffic to real mobile traffic.

In this and our previous works [60, 61], delta-sigma modulation shows high BW efficiency, i.e., it only consumes small fronthaul capacity per unit of BW of LTE signals. On the other hand, CPRI-based solutions offer small EVM and high SNR, and therefore can support higher modulation and larger net information rate, so bit efficiency is introduced as a second metric. Although delta-sigma modulation has high bandwidth efficiency, its bit efficiency gain will not be as high as its bandwidth efficiency gain due to the high EVM and low modulations. In Table 4, it is assumed that all CPRI-based solutions carry the modulation of 1024-QAM. So far, the best bandwidth efficiency was achieved by delta-sigma modulation [60, 61], which was implemented by offline processing. The highest bit efficiency was achieved by our previous work [18, 19] using statistical compression of CPRI. Figure 13 illustrates the bandwidth and bit efficiencies of different solutions.

Table 4 – Comparison of Bandwidth/Bit Efficiencies of CPRI, CPRI-Compression, and Delta-Sigma Modulation

NGFI	CPRI-based solutions			Delta-sigma modulation				
	CPRI	Statistical Compression	Lloyd compression					
References	[9]	[18, 19]	[20]	[60]	[61]	[61]	This work	
Order	N/A			2	4	4	4	4
Sampling rate (MSa/s)	30.72	23.04	30.72	10,000	10,000	10,000	5,000	5,000
Bits	15[1]	8	8	1	1	2	1	1
Fronthaul data rate (Gbps)	0.9216	0.36864	0.49152	10	10	20	5	5
LTE carrier #	1			32	32	32	10	14
LTE bandwidth (MHz)	18			576	576	576	180	252
Modulation	1024			64*18 16*14	256*16 64*16	1024*10 256*22	1024*4 256*6	1024*2 256*4, 64*8
Net information data rate (Gbps)	0.18			2.952	4.032	4.968	1.584	1.8
Bandwidth efficiency (MHz/Gbps)[2]	19.5	48.8	36.6	57.6	57.6	28.8	36	50.4
Bandwidth efficiency gain w.r.t. CPRI	1	2.5	1.875	2.95	2.95	1.48	1.85	2.58
Bit efficiency[3]	0.195	0.488	0.366	0.295	0.403	0.248	0.317	0.36
Bit efficiency gain w.r.t. CPRI	1	2.5	1.875	1.51	2.07	1.27	1.63	1.85

[1] CPRI uses 15 quantization bits and one control bit for each sample, and exploits line coding of 8b/10b or 64b/66b [9]. For a fair comparison, there is no control bit or line coding considered.
[2] Bandwidth efficiency = fronthaul data rate / LTE bandwidth, which measures the required fronthaul capacity per unit of bandwidth of LTE signals.
[3] Bit efficiency = fronthaul data rate / net information data rate, which measures the mapping efficiency between the fronthaul traffic and mobile traffic.

Table 5 gives a comparison of various LLS options. Although the proposed option 9 splits at a lower level than option 8, it has improved bandwidth/bit efficiency and reduced fronthaul data traffic than CPRI. Compared with higher level split options 6, 7, and 8, it exploits an all-digital RF transceiver, centralizing high-RF layer at DU, replacing conventional DAC by a low-cost BPF, and eliminating the need of local oscillator and mixer at RRU. It not only makes low-cost, low-power, and small-footprint cell sites possible for small cell deployment, but also paves the road toward SDR and virtualization of DU/RRU for improved compatibility and reconfigurability among multi-RATs. Since option 9 splits deep in the RF layer, it has

very stringent latency requirement, which demands highly deterministic latency and makes it suitable for radio coordination applications.

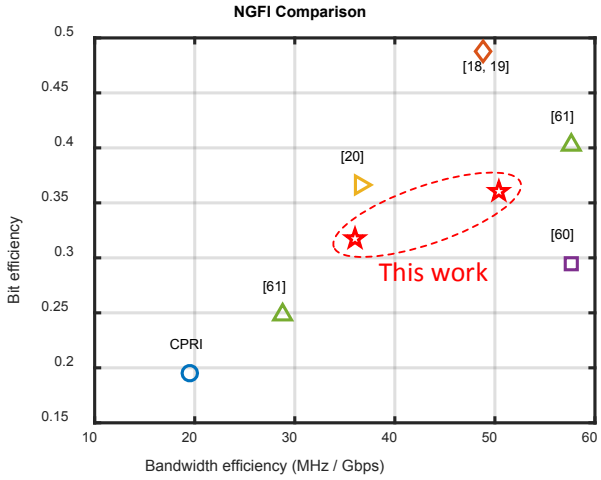

Figure 13 - Comparison of bandwidth/bit efficiencies of CPRI, CPRI compression, and delta-sigma modulation.

Table 5 – Comparison of Various Low Layer Split (LLS) Options

3GPP / CPRI cooperation		6/D	7.3/I_D	7.2/II_D, I_U	7.1	8 (CPRI)/E	9
Architecture		Most distributed	More centralized on the right				Most centralized
RRU functions		PHY + RF layers	Low-PHY + RF layers			RF layer	Low-RF layer
RRU complexity		Highest	Medium (higher on the right)			Low	Lowest
		Complete RF layer implemented in analog domain at RRU, including DAC, LO, mixer					Only need PA and BPF
NGFI data		Baseband bits	Scrambled bits	Frequency domain I/Q samples		Time domain I/Q samples	Bits after ΔΣ modulation
Data rate		Lowest	1/10 of CPRI (higher on the right)			Highest	1/4~1/2 of CPRI [60, 61]
Data rate scalability		Traffic dependent Antenna independent, scale with MIMO			Traffic independent Antenna dependent, scale with antenna		
Ethernet compatibility	802.1CM	Future amendment	Class 2			Class 1	Future amendment
	P1914.1	Support	Support			N/A	N/A
	P1914.3	N/A	Structure-agnostic encapsulation Native RoE mapping			Structure-aware encapsulation Native RoE mapping	Structure-agnostic encapsulation
Latency requirement		Lowest	Higher latency requirement on the right				Highest

There are several IEEE standards addressing the Ethernet compatibilities of LLS options [66-68], shown in Table 5. As a collaborative effort of CPRI cooperation and IEEE 802.1 working group, IEEE 802.1CM specifies time sensitive network (TSN) profiles for fronthaul traffic over Ethernet bridged networks [66, 67]. Currently it supports two function split options, Class 1 for CPRI and Class 2 for eCPRI, and can address other split options, such as option 9, by future amendment. IEEE P1914.1, standard for packet-based fronthaul transport networks, defines the architecture and requirements of Ethernet-based mobile fronthaul traffic [68], including the Ethernet packetization of option 6 and 7. IEEE P1914.3 (previously P1904.3), standard for radio over Ethernet (RoE) encapsulations and mappings, defines 3 encapsulation methods of radio data into Ethernet packets [68], including structure-aware encapsulation, structure-agnostic encapsulation, and native RoE mapping. Structure-aware encapsulation maps CPRI frames to/from Ethernet frames with the help of knowledge of CPRI frame structure. It is optimized for CPRI and allows

CPRI to be structurally remapped to RoE. Structure-agnostic encapsulation offers a simple tunneling of radio data stream without knowledge of its frame structure, which is not restricted to CPRI and can support option 9. The third encapsulation method, native RoE mapping maps IQ payload data directly to Ethernet packets, and can support IQ samples from either time domain, such as option 8 (CPRI), or frequency domain, such as eCPRI or option 7.1, 7.2.

One major challenge to all-digital transceiver and SDR is the high processing speed. Delta-sigma modulation requires high oversampling ratio to achieve satisfying SNR/EVM performance. Moreover, digital frequency up-conversion needs a clock rate four times of the carrier frequency. To circumvent the speed limit of existing CMOS or FPGA, several parallel processing techniques have been reported, including polyphase decomposition [44, 45] and look-ahead time-interleaving [47, 48]. In this paper, for a concept-proof experiment, only basic pipeline technique is used. Given the wide frequency range of 5G from sub-1 GHz to millimeter wave, and various scenarios, e.g., eMBB, uRLLC, and mMTC, the proposed option 9 function split is expected to first find its applications in low frequency radio coordinate scenarios, such as low band 5G (T-Mobile 600 MHz). Given its highly deterministic latency, it also has high potential in uRLLC. By leveraging the low-cost, low-power, and small-footprint cell site enabled by all-digital RF transceiver, option 9 split can also be used to support low frequency narrowband IoT (NB-IoT) applications.

Conclusion

In this paper, we propose and demonstrate a new NGFI function split option 9 based on all-digital RF transceiver using delta-sigma modulation. Different from other low layer split options, e.g., 6 (MAC-PHY), 7 (high-low PHY), and 8 (CPRI), the proposed option 9 exploits the design of all-digital RF transceiver and splits functions within the RF layer, with high-RF layer centralized in DU, and low-RF layer left in RRUs. A proof-of-concept all-digital RF transmitter of LTE/5G signals is experimentally demonstrated using real-time bandpass delta-sigma modulation implemented with a Xilinx Virtex-7 FPGA. The delta-sigma modulator works at 5 GSa/s and can encode LTE/5G signals with bandwidth up to 252 MHz and modulation format up to 1024-QAM to a 5Gb/s OOK signal, which is transmitted from DU to RRU over 30-km fiber. To relax the FPGA speed requirement, a 32-pipeline architecture is designed for parallel processing. Four experimental cases are presented to validate the feasibility of proposed option 9, and 5G two-carrier aggregation and LTE 14-carrier aggregation are successfully demonstrated with the EVM performance satisfying the 3GPP requirement. A detailed comparison between CPRI, CPRI compression, and deltas-sigma modulation, in terms of bandwidth and bit efficiencies is also presented.

Although it splits at a lower level than option 8, the proposed option 9 offers improved efficiency than CPRI and reduces the fronthaul traffic. Compared with higher level split option 6, 7 and 8, it exploits a centralized architecture with most RF layer functions consolidated in DU, eliminating DAC, LO, and mixer at RRU, and enables a low-cost, low-power, and small-footprint cell site for small cell deployment. Moreover, all-digital RF transceivers pave the road toward SDR and virtualized DU/RRU for multi-RAT compatibility, which has high potential in mMTC and NB-IoT applications. Given its deterministic latency, it is expected that the proposed option 9 split is more suitable for radio coordination applications than other higher level split options.

In the future, to target wider signal bandwidth and higher carrier frequency of 5G signals, more efficient time-interleaving pipeline processing architecture need to be investigated to relax the FPGA speed. Moreover, higher-order delta-sigma modulator with advanced noise shaping techniques, such as multiband operations for non-contiguous carrier aggregation or multi-RAT coexistence, will be investigated as well.

Appendix

1. State-of-the-Art of Delta-Sigma Modulator

Table 6 lists a state-of-the-art of delta-sigma modulators implemented by either CMOS or FPGA, including lowpass [30, 32-34, 36-39, 41-45, 47, 48], bandpass [31, 35], and multiband [40, 49-52] modulators. To relax the FPGA speed requirement, several time-interleaving or parallel processing architectures have been presented [38, 39, 43-45, 47, 48]. Figure 14 shows a summary of all-digital transmitters in terms of sampling rate and signal bandwidth. The right panel shows an overall summary; whereas the left panel (green circles) zooms into the early results with low sampling rate and signal bandwidth.

Table 6 - State-of-the-Art of All-Digital Transmitter based on Delta-Sigma Modulation

Reference	Sampling rate (GSa/s)	Bandwidth (MHz)	Fc (GHz)	Signal band	Implementation	Pipeline #	Signal type
[30]	0.0352	1.1	Baseband	Lowpass	CMOS 0.5 µm	1	Continuous time Tx
[31]	0.7	< 1	0.175	Bandpass	CMOS 130 nm	1	GSM
[32]	2.625	200	5.25	Lowpass	CMOS 130 nm	1	Digital RF Tx
[33]	<3.6	10, 20	2.4-3.6	Lowpass	CMOS 90 nm	1	Digital RF Tx
[34]	5.4	5.6, 11.2, 20	2.4-2.7	Lowpass	CMOS 65 nm	1	Wi-Fi, WiMAX
[35]	2.6, 4	Up to 50	0.05-1	Bandpass	CMOS 90 nm	1	Digital RF Tx
[36]	0.05	0.25, 0.5	Baseband	Lowpass	Altera Stratix	1	OFDM, CDMA
[37]	0.045	1.25/1.23	2.45, 1	Lowpass	Altera Stratix	1	WiMAX, CDMA, EDGE
[38]	0.64, 0.8	3.84/7.68 (LTE) 4/8 (WiMAX)	2.1, 2.5	Lowpass	Altera Stratix II GX	8	WiMAX, LTE
[39]	0.025	1.6	1	Lowpass	Unknown FPGA	4	CDMA
[40]	3.9	5+5	0.8, 1.5	Dual-band	Unknown FPGA	1	Dual-band LTE
[41]	0.225	1.25+1.5	0.45, 0.9	Lowpass	Xilinx Virtex 6 HX380T on ML628	1	Dual-band WiMAX + SC-QAM[1]
[42]	0.15625	1.25+1.5	1.25, 0.78125	Lowpass	Xilinx Virtex 6 HX380T on ML628	1	Dual-band SC-64QAM + WiMAX
[43]	1/0.9 (1st/2nd order)	Up to 12.5	1, 0.9	Lowpass	Xilinx Virtex 6 HX380T on ML628	4	Single-carrier
[44]	3.2	6.1-122	1.6	Lowpass	Xilinx Virtex 6 VHX280T on ML628	16	Single-carrier
[45]	3.2	6-120	3.2	Lowpass	Xilinx Virtex UltraScale XCVU095 on VCU1287	16	Single-carrier
[46]	0.7	5	0.7	Envelope	CMOS 90 nm	1	LTE
[47]	10.4 = 0.325 * 32	20	5.2	Lowpass	Xilinx UltraScale XCVU095 on VCU108	32	Wi-Fi 802.11a
[48]	9.6 = 0.3 * 32	488	4.8	Lowpass	Xilinx UltraScale XCVU095 on VCU108	32	SC-64QAM
[49][3]	6.25	20+20	0.856, 1.45	Dual-band	Simulation + AWG[2]	1	Dual- band LTE

Reference	Sampling rate (GSa/s)	Bandwidth (MHz)	Fc (GHz)	Signal band	Implementation	Pipeline #	Signal type
[50]	6.25	10+20	0.874, 1.501	Dual-band	Simulation + AWG	1	Dual-band LTE
[51]	2.15	5+10	0.244, 0.5	Dual-band	Simulation + AWG	1	Dual-band LTE
[52]	7	10+10+10	0.71, 1.75, 2.51	Triple-band	Simulation + AWG	1	Triple-band LTE
This work	5	99-252	0.96	Bandpass	Xilinx Virtex-7 VX485T on VC707	32	5G, LTE carrier aggregation

[1] SC-QAM: single-carrier quadrature amplitude modulation
[2] AWG: arbitrary waveform generator
[3] The performance of references [30-48] are illustrated in Fig. 14. References [49-52] are not included since they are not implemented by CMOS or FPGA, but by offline processing.

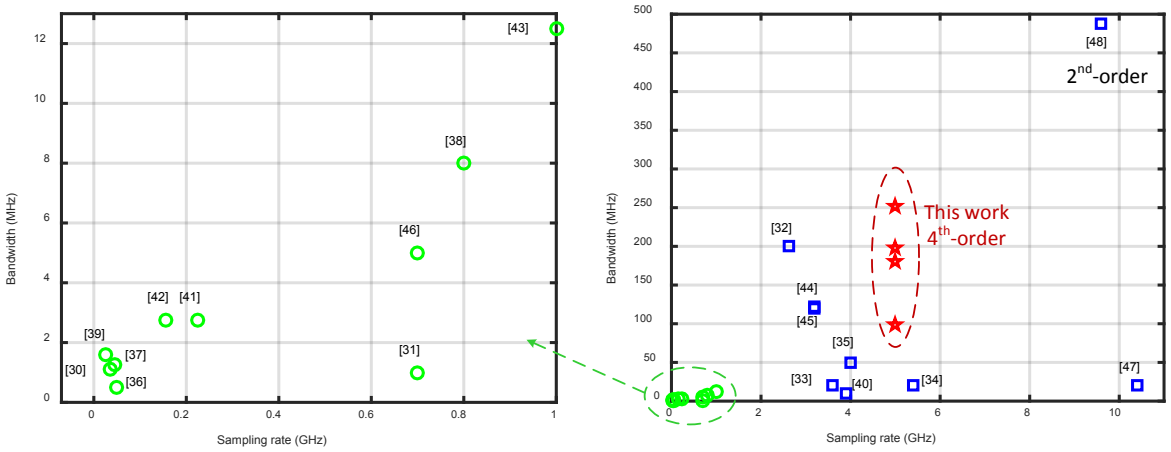

Figure 14 - State-of-the-art of delta-sigma modulator for all-digital RF transmitter.

In [48], a high speed lowpass delta-sigma modulator was demonstrated with 9.6 GSa/s sampling rate and signal bandwidth of 488 MHz. To accommodate this high speed, 32-pipeline FPGA architecture was used with 300-MHz clock rate in each line. This is the fastest delta-sigma modulator reported so far, but with only second-order modulation. In this paper, we present a fourth-order bandpass delta-sigma modulator with 5 GSa/s sampling rate and 252 MHz signal bandwidth. A 32-pipeline architecture was also employed with clock rate in each pipeline of 156.25 MHz. So far this is the fastest four-order modulator reported.

Abbreviations

ADC	analog-to-digital converter
AWG	arbitrary waveform generator
BBU	baseband unit
BPF	bandpass filter
BS	base station
CPRI	common public ration interface
C-RAN	centralized/cloud-RAN
CRFF	cascaded resonator feedforward
CU	central unit
DAC	digital-to-analog converter

DOCSIS	data over cable service interface specification
DSO	data storage oscilloscope
DU	distributed unit
eMBB	enhanced mobile broadband
EPC	ethernet packet core
EVM	error vector magnitude
FDM	frequency division multiplexing
FIFO	first-in-first-out
FMC	FPGA mezzanine card
HLS	high layer split
HPC	high-pin count
IoT	internet of things
LLS	low layer split
LO	local oscillator
MAC	media access control
mMTC	massive machine type communication
MEC	mobile edge computing
MGT	multi-gigabit transceiver
Multi-RATs	multiple radio access technologies
NB-IoT	narrowband IoT
SC-QAM	single-carrier quadrature amplitude modulation
SDR	software defined radio
PA	power amplifier
NGFI	next generation fronthaul interface
NG-RAN	next generation-radio access network
OSR	oversampling rate
PDCP	packet data convergence protocol
PHY	physical
PON	passive optical network
RAN	radio access network
RAT	radio access technology
RF	radio frequency
RLC	radio link control
RoF	radio-over-fiber
RRC	radio resource control
RRH	remote radio head
RRU	remote radio unit
TDM	time division multiplexing
uRLLC	ultra-reliable low latency communication

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