

TIME SCHEMES IN REMOTE PHY ARCHITECTURE

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Abstract

The Remote DOCSIS Timing Interface (R-DTI) is the timing specification standardized recently for R-PHY architecture. R-DTI leverages on IEEE1588v2 with a special profile for DOCSIS applications. This paper explains how R-DTI works and what are the requirements on the time/frequency synchronization between CCAP core and RPD to ensure proper DOCSIS operations. Two operation modes that are defined in R-DTI, the Node_Slave mode and Node_Master mode, are explained and their operations are illustrated. Tests are done in Cisco R-PHY Lab to validate R-DTI under various network conditions. Test results show that, with the commercial R-DTI solutions, the timing and frequency synchronization between CCAP core and RPD can be achieved within 5 minutes in all the test cases and CM can operate normally without any performance degradation after the synchronization is achieved.

INTRODUCTION

Remote PHY (R-PHY) has been defined in Modular Headend Architecture v2 (MHA v2) (reference 1). It promises higher capacity and lower operation cost by moving the PHY from the CCAP at headend to the optic node and connecting CCAP core and node through digital fiber. The connection between the node and CM is still DOCSIS and over coaxial, but with much short distance. This results in improved signal quality and reduced OPEX. The specifications of R-PHY architecture have been standardized by CableLabs and participating vendors (reference 2).

Since PHY locates in optic node, separated from CCAP core, timing/frequency synchronization are required between node and core to ensure proper operation. The conventional DOCSIS DTI timing is not appropriate for R-PHY application. CableLabs R-PHY specification has defined R-DTI (remote DOCSIS timing interface) as the timing protocol for the timing/frequency synchronization between CCAP core and node in R-PHY architecture. It leverages the IEEE 1588-2008 (1588v2) protocols and defines specific profile for DOCSIS R-PHY application (reference 3).

Deploying 1588v2 in R-PHY architecture meets with lots of challenges due to the stringent timing/frequency sync requirements of DOCSIS PHY, MPEG video and OOB (out-of-band) signals. In this paper, we introduce the timing scheme in R-PHY architecture: what are the timing/frequency synchronization requirements for CCAP core and node to support various services (data, video, and OOB), how 1588v2 works in R-PHY architecture, and what the design challenges and solutions are. Also include are the Lab test data on R-DTI performances.

TIME/FREQUENCY SYNCHRONIZATION REQUIREMENTS

Figure 1 shows the simplified R-PHY architecture emphasizing the Remote DOCSIS Timing Interface (R-DTI). In R-PHY architecture, the PHY of CCAP is moved to the node, called as R-PHY device (RPD), and the rest of the CCAP is called CCAP core. CMTS core and the RPD are usually located in two different physical

locations, and their operations require they synchronize in both timing and frequency. Timing and frequency synchronization between CCAP core and RPD are achieved through the precision time protocol (PTP, IEEE 1588v2) as defined in R-DTI.

The requirements for timing and synchronization of the DOCSIS system come from the following areas:

- 1) DOCSIS physical level timing requirements
- 2) Time/frequency synchronization between CCAP core and R-PHY device (RPD)
- 3) Precision timing services like mobile backhaul, FCC911

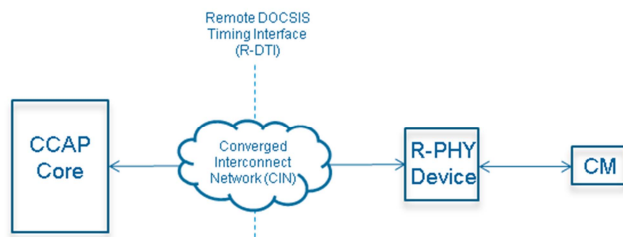


Figure 1. High level R-PHY Architecture

Figure 2 shows the R-PHY's clocking architecture. The time and frequency recovered from the 1588 DPLL/NCO will drive the DS PHY and US PHY. It should meet the clock quality specifications as follows.

- Physical level requirements of DOCSIS 3.0/3.1 PHY, EQAM, OOB and NDF/NDR:
 - DOCSIS reference clock (10.24MHz or 204.8MHz)
 - Accuracy: +/-5ppm
 - Jitter or phase noise: DOCSIS DRFI spec for D3.0 and PHY spec for D3.1
 - Frequency drift rate: 10ppb per second for DOCSIS data
 - 10ppm per hour for QAM video

- Time
 - Time jitter: SYNC jitter must be less than 500ns (DOCSIS 3.0)
- Time/frequency synchronization between CCAP core and RPD
 - Accuracy requirements: time +/- 1ms; frequency: +/- 200ppb
- Precision timing services like mobile backhaul, FCC-911
 - These requirements are product specific. R-PHY system could use DTP protocol to support advanced timing services.

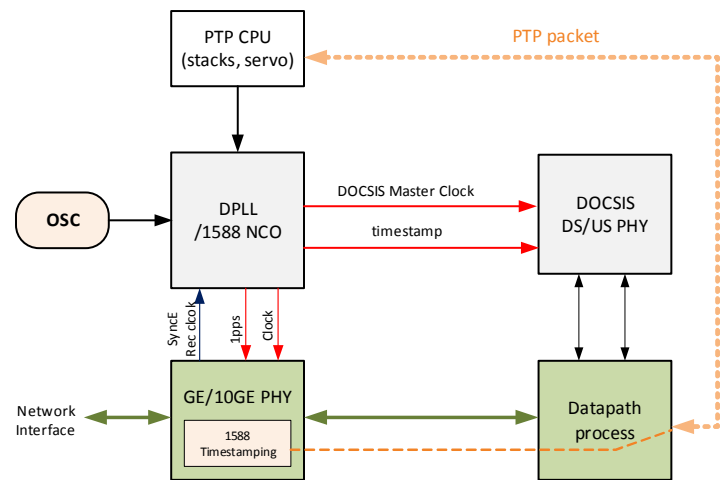


Figure 2. R-PHY Clocking Architecture

HOW 1588v2 WORKS IN R-PHY NETWORK

R-DTI adopts IEEE 1588v2 with a frequency and time & phase profile customized for R-PHY applications. IEEE 1588v2 provides time synchronization between two nodes across a packet network without mandating all intermediate nodes being replaced, hence becomes the best tool for the R-DTI implementation. There are two operation modes defined in R-PHY architecture.

1) Node_Slave operation mode

Figure 3 is the timing architecture for the Node_Slave operation mode. RPD acts as the timing slave, and its clock is driven by an external master clock. The master clock may collocate with the CCAP core, thus the CCAP core provides with the master clock (figure 3(a)), or in general, the master clock locates in the cloud, and the CCAP core itself is a slave to this network based grand master (GM) as well (Figure 3(b)). In the latter case, the CCAP core will be a Boundary Clock: it acts as a slave synchronized to the network GM but serves as the master clock to the RPD. In both cases, in the Node_Slave mode, RPD always acts as an Ordinary Clock (OC) synchronized to the master clock coming from CCAP core. This will ensure all network devices (RPDs and the CCAP core) have a single clock source which could be derived from the network 1588 GM. DOCSIS operation requires all devices are in a single clock domain.

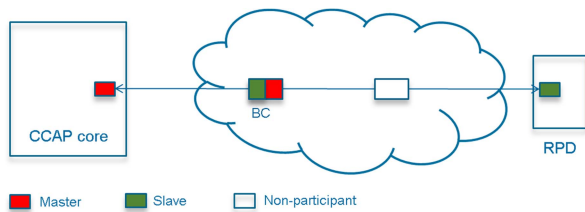


Figure 3(a). Master clock located with CCAP core

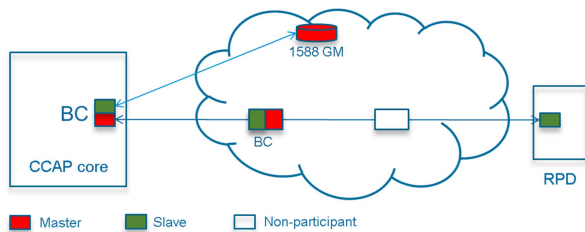


Figure 3(b). Network based 1588 GM

Figure 4 shows the basic synchronization message exchanges in the Node_Slave operation mode. It is evident that the time and frequency synchronization are achieved by the 1588 client located in RPD, as specified in IEEE 1588v2 (reference 4).

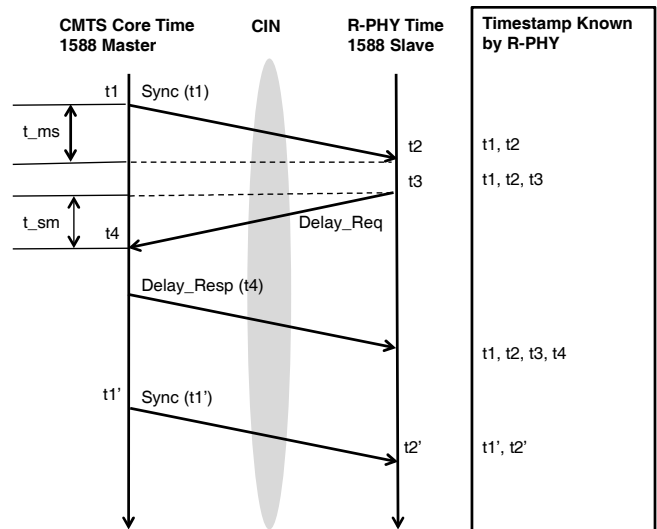


Figure 4. Synchronization message exchanges in the Node_Slave operation mode

2) Node_Master operation mode

The other operation mode defined in R-DTI is the Node_Master mode. Shown in Figure 5 is the timing architecture for the Node_Master operation mode.

In the Node_Master operation mode, the R-PHY acts as a 1588 Master, while CMTS Core acts as a 1588 Slave.

In this mode, the CCAP core needs to generate multiple clock islands, one for each RPDs that it connects to. The RPD distributes its frequency and phase information through 1588 synchronization messages.

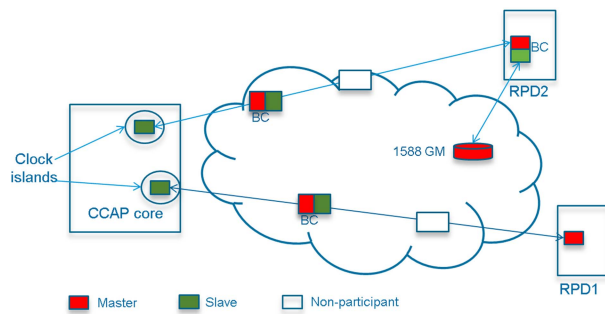


Figure 5. Operation Mode – Node_Master

CMTS Core obtains the frequency and phase information from the synchronization messages and runs a phase calibration process to track the RPD time and frequency. The timing and frequency information for each RPD will be kept in the clock island corresponding to that RPD. Any messages to a RPD (for example, MAC scheduling) with timing stamps will be sent out with the ‘local timing’ in its corresponding clock island.

The local timings in the clock islands need be updated continuously through IEEE 1588 messages. Figure 6 shows the basic synchronization message exchanges in this case between the CCAP core and the RPD. In this case the time and frequency synchronization are achieved by the 1588 client located in CCAP core.

Please note: in this case, the local clock and timing at the CCAP core will not be adjusted to synchronize with any particular RPD. The timing/frequency synchronization between CCAP core and RPDs are logic through the clock islands.

In the Node_Master operation mode, the local clock at RPD may be in a free run mode with an internal clock source such as an oscillator, or RPD may synchronize to a 1588 GM in the network. In the latter case, the R-PHY act like a 1588 BC – it is a slave clock to the 1588 GM in the network and acts like a master

clock to the CCAP Core. As described before, the local clock at the CCAP core does not need be adjusted to synchronize to the RPD, as the clock synchronization between CCAP core and RPD are logic and through the clock islands in this Node_Master operation mode. The CMTS core may be in a free run mode or synchronized to an external clock source rather than RPD’s.

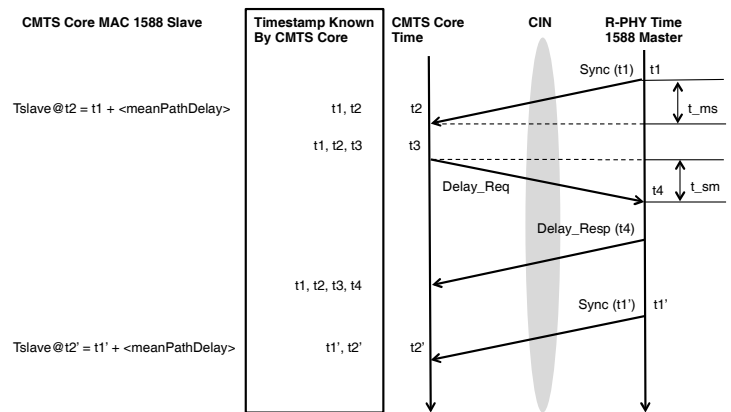


Figure 6. Synchronization message exchanges in the Node_Master operation mode

R-DTI specifies the RPDs must support both Node_Slave and Node_Master operation modes. The CCAP core must support the Node_Slave mode, and may support the Node_Master mode.

IEEE 1588 PROFILE FOR R-PHY

IEEE 1588v2 provides time synchronization between two nodes across a packet network without mandating all intermediate nodes being replaced, hence becomes the best tool for the R-DTI implementation. The accuracy requirements of the PTP synchronization are application-dependent. Sub-microsecond accuracy is required for typical telecom applications (3G/LTE, etc.). The accuracy requirements for DOCSIS operations are much lower (see the next paragraph).

Therefore, R-DTI leverage the existing IEEE-1588v2 protocol but with tailored profile for DOCSIS applications. In other words, R-DTI is a specific 1588 profile for DOCSIS R-PHY application. The same PTP stacks and hardware components can be used at both master and client sides. Often, the R-DTI client has the capability to be configured to operate in two different modes: a) DOCSIS R-PHY Mode; b) Advanced Timing Mode.

1) DOCSIS R-PHY mode

In this mode, the profile definition considers the timing and frequency requirements for proper operation of DOCSIS, video, OOB, and NDF/NDR in R-PHY architecture. Precisely, the 1588 profile for R-PHY calls for the following requirements:

- Phase alignment $\leq 1\text{ms}$
- Frequency accuracy $\leq \pm 5\text{ppm}$
- Frequency drift $\leq 10\text{ppb/s}$ and 10ppm/hr
- Phase jitter $< 500\text{ns}$
- Lock time from cold start < 5 minutes
- Worst time and frequency offset between two nodes (cold start): 10ppm in frequency, and arbitrary time offset in time

These requirements are customized for R-PHY application, ensuring proper DOCSIS operations.

When IEEE 1588 client is used in R-PHY (either at CCAP core or RPD), its servo algorithm should be tailored for this RPHY profile. The timing and frequency synchronization should be realized in two phases: the initial acquisition phase where the phase, frequency can be adjusted arbitrarily, and the steady phase where disruptive time adjustment shall not be allowed, and the frequency adjustment slope shall be less than 10ppb/s (and 10ppm/hr). The acquisition phase shall be completed in less than 5 minutes, as illustrated in Figure 7.

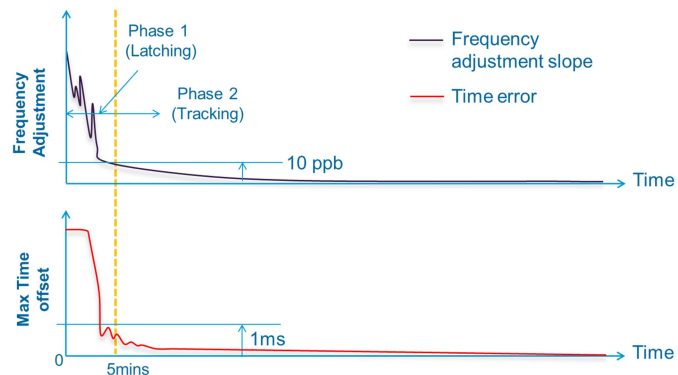


Figure 7. IEEE 1588 client servo algorithm in two phases.

2) Advanced Timing Mode

In the advanced timing mode, the output clock quality could be significantly improved to meet the mobile backhaul or DTP requirements. As such the servo could require a much longer time to converge, leading a much longer clock settle time.

SIMULATION AND TEST RESULTS

To evaluate timing and frequency synchronization performances of R-DTI in various CIN scenarios, commercial R-DTI solutions have been tested in Cisco R-PHY Lab. Figure 8 and Figure 9 show the two test setups. Test Setup-A is for testing R-DTI client performance under various CIN conditions. Different CIN conditions are modelled with different network PDV. In Setup-B, the recovered time and frequency out of the R-DTI client evaluation board were fed into the DOCSIS 3.0 R-PHY node. The purpose of test Setup-B is for evaluating the impact of R-DTI on actual R-PHY operations.

1) Test Setup A

Equipment used in test Setup-A includes:

- PTP client evaluation board from R-DTI solution vendors. The servo algorithm is specific for R-DTI
- 1588v2 grand master, TP-5000
- Calnex's Paragon-X, it is used for simulating the PDV of CIN and measuring the recovered clock quality
- Raken TCXO E6615LF on the PTP evaluation board

2) Setup B

Setup-B is based on Setup-A but contains additional equipment for evaluating the impacts of R-DTI on R-PHY operation:

- Cisco R-PHY system, includes uBR10K, R-PHY node(CMC), and cable modems
- IXIA for simulation of the user traffic
- Switches for connecting CMTS core, R-PHY, and IXIA

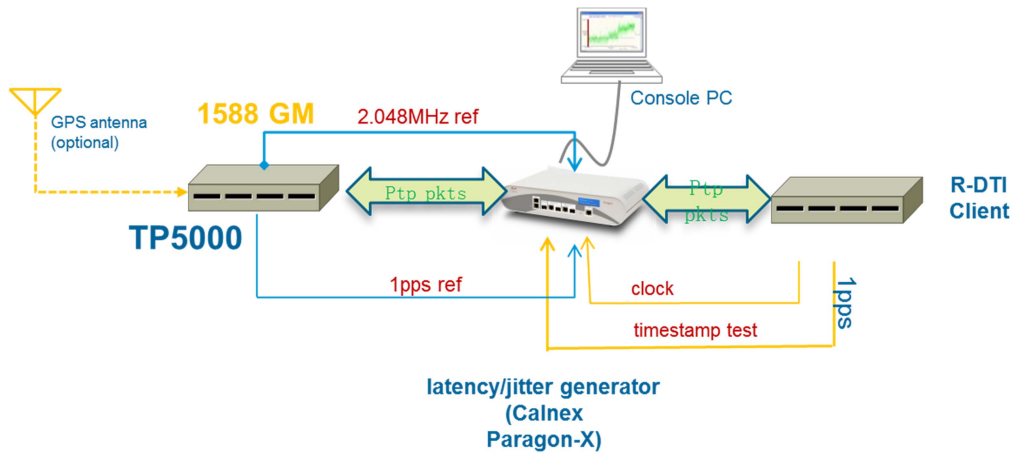


Figure 8. Test Setup-A

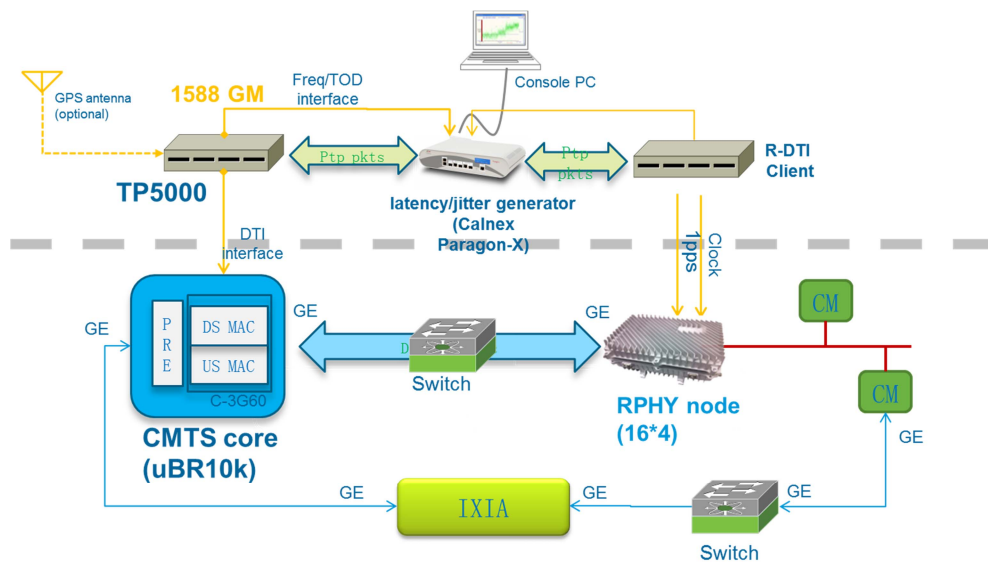


Figure 9. Test Setup-B

In both test Setup-A and Setup-B, R-DTI is configured as follows:

- 1-step 1588, unicast, 16pps sync packet rate
- R-DTI profile in PTP evaluation board

3) R-DTI Test results with Setup-A

Test cases in Setup-A were created to provide sufficient coverages on network conditions and address some key issues with R-DTI. As IEEE 1588 servo algorithm is tailored for R-PHY application, which has a much relaxed timing accuracy requirement compared to typical telecom applications, one expects much faster timing and frequency convergences in all test cases. Calnex Paragon-X is used to simulate various CIN network conditions through various packet delay variation (PDV), and the time/frequency synchronization performances in different phases are measured for each of the test cases.

The simulated networking conditions covered:

- Gaussian random packet delay variation with different peak, mean, or variation
- Symmetric & asymmetric delay between master and client
- Different traffic load, link re-route, random noise, network congestions, dynamic floor/mean delay
- 1x, 10x, 20x, 50x, 100x of ITU-T reference PDV pattern of Metro Ethernet, defined in G.8261 TC12~17
- Measured PDV data from some service providers' network
- Measured PDV data from Cisco routers
- RPD using R-DTI synchronization in different work status

Table 1 lists all the test cases, and the convergence times and time/frequency accuracies achieved after the time/frequency lock is declared in each case.

Table 1. Test Cases

TC#	Description	Lock time (s)	Time error after lock (us)	Frequency offset after lock (ppb)
1	Symmetric PDV, Gaussian p2p 5ms	240	179	359
2	Symmetric PDV, Gaussian p2p 10ms	240	171	601
3	Asymmetric PDV, -uplink Gaussian p2p 10ms -downlink Gaussian p2p 7ms	240	138	617
4	Dynamic and asymmetric PDV -uplink Gaussian p2p 10-7-5ms -uplink Gaussian p2p 2-2-2ms	240	343	587
5	Dynamic and asymmetric PDV -uplink Gaussian p2p 7-5-3ms -uplink Gaussian p2p 2-1-2ms	240	285	1134
6	Dynamic and asymmetric PDV with variable floor and mean delay	240	407	816
7	G.8261 TC12-17, 1 times magnitude	240	233	726
8	G.8261 TC12-17, 20 times magnitude	240	193	715
9	G.8261 TC12-17, 100 times magnitude	240	615	1645

10	Operator A tested PDV data	240	4	18
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It is evident that the R-DTI client can converge and meet the R-DTI timing and frequency accuracy requirements within 5 minutes for all the test cases. Please note: some of the test cases render very disruptive CIN conditions and could be considered as worst cases. In all the test cases, the initial frequency offset is set to 10ppm, the worst case per DOCSIS specification. When the lock is declared (within 5 minutes), the servo still works to improve the timing and frequency accuracy but with no disruptive time adjustment (phase jump) and caps the frequency adjustment slope to less than 10ppb/s. Figure 10 and Figure 11 show the time and frequency converge process for some of the test cases.

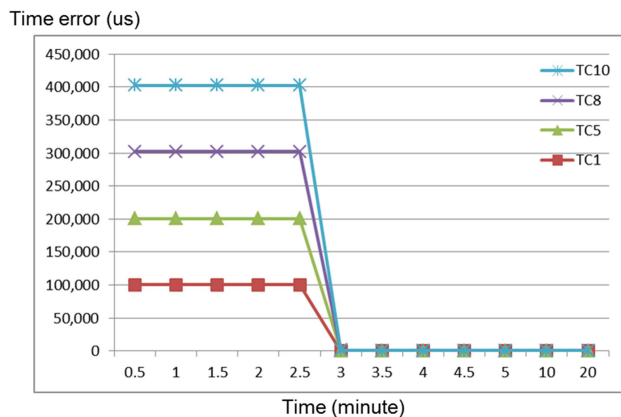


Figure 10. Timing errors with time

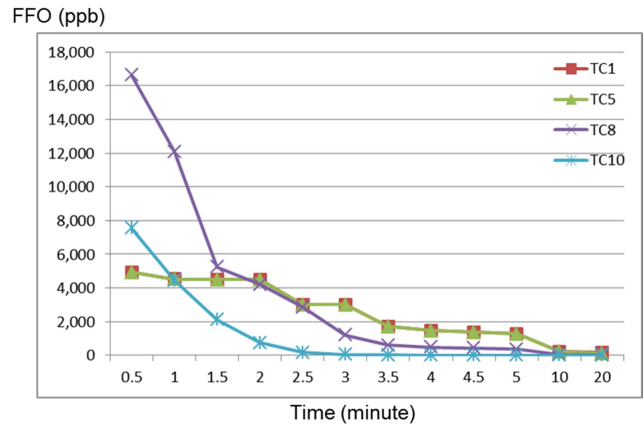


Figure 11. Frequency errors with time

3) Test results in Setup-B

With Setup-B, the impacts of R-DTI on actual R-PHY system operation are evaluated. The same test cases used for Setup-A are used for test Setup B. The evaluation metrics include the following items:

- phase noise of the local clock with the reference clock driven by the recovered clock via R-DTI
- CM initialization
- CM throughput and latency
- Timing holdover during clock outage/glitch
- Timing and frequency convergence during PTP SW restart (warm-restart/switchover).

a) Phase noise

DOCSIS DS/US has stringent requirements on reference clock's phase noise. To meet the phase noise requirement, an external VCXO is required. This VCXO is then driven by a reference input that comes from the recovered clock via R-DTI.

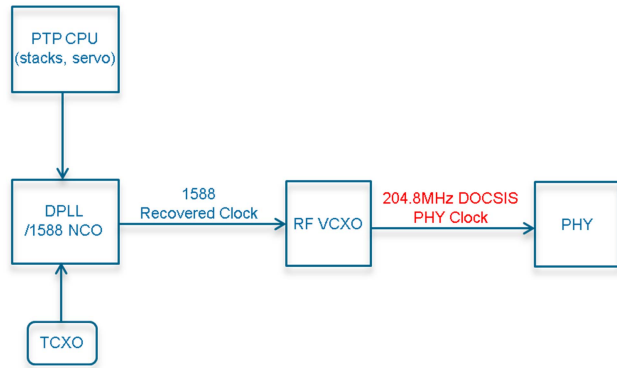


Figure 12. RF reference clock from R-DTI

Figure 12 show the clock architecture. The phase noises are measured for both R-DTI acquisition stage (before lock) and steady stage (after lock), and the measurement results are shown in 13 and 14. Compared to the phase noise performance of the VCXO with a ‘good’ reference clock, the phase noise performance of the clock driven by the recovered clock via R-DTI has no degradation after the lock is declared; indicating that the R-DTI has little impacts on the phase noise performance of VCXO after the lock is achieved. There are some slight degradations on phase noise in the frequency range below 60Hz in the acquisition stage. This wouldn’t be an issue as the system is not expected to start normal operation in the acquisition stage. Moreover, phase noise below 60Hz has little impacts on system performance and is not even specified in DOCSIS PHY specs.

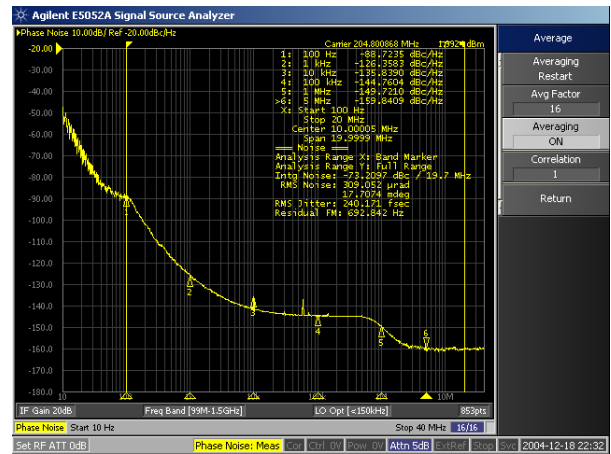


Figure 13. RF VCXO output clock phase noise during 1588 acquisition

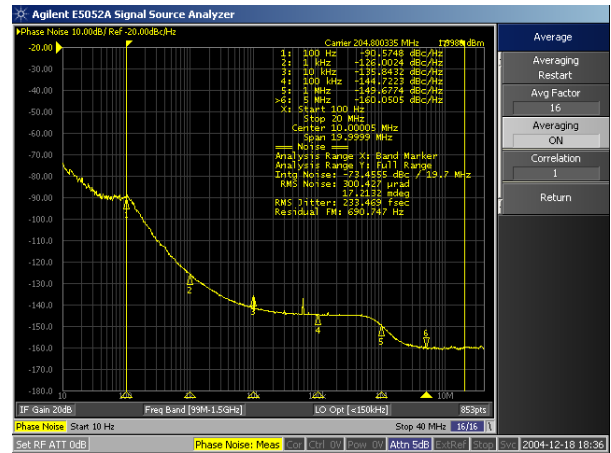


Figure 14. RF VCXO output clock phase noise after 1588 lock declared

It is evident that the phase noise of the RF reference clock is stable and can meet DOCSIS requirements after the 1588 client lock is declared (5 minutes after power up).

b) CM initialization

There are no visible differences observed on CM initialization once the time/frequency lock is declared on RPD.

c) CM throughput and latency

Compared with I-CMTS system, there are no visible differences of the throughput and latency observed with the same test conditions once the time/frequency lock are declared on RPD.

d) Timing holdover

Test the R-DTI client holdover capability during clock outage/glitch by disrupting 1588 link of RPD on purpose. It is observed that CM can continue work properly for up to 1.5 hours with typical commercial TCXO.

e) Timing and frequency convergence during PTP SW restart (warm-restart/switchover)

There are no visible impacts observed on CM performances during PTP SW restart (warm-restart) or PTP GM switch, the output time/frequency keeps stable without any visible differences on performance.

SUMMARY

Lab tests on R-DTI performances have been completed for various CIN conditions in Cisco R-PHY Lab. The CIN conditions are modeled with different network PDV through the network emulator (Calnex's Paragon-X). Test results show that commercial R-DTI solutions can achieve timing and frequency converge within 5 minutes under all the test conditions and with arbitrary initial phase offsets. After the convergence, the timing and frequency accuracies meet the requirements specified in R-DTI specs and ensure proper DOCSIS operations. Little impacts are observed on RF VCXO clock phase noise once the time/frequency lock is declared (within 5 minutes). No visible differences are observed on CM throughput and latency once the time/frequency is converged.

With a typical TCXO, once the time/frequency are converged, R-DTI has the capability to maintain the required timing and frequency accuracy for up to 1.5 hours without a single 1588 messages exchanges. This capability will ensure the continuous normal DOCSIS operation during 1588 link outage/glitch (1588 GM switchover, clock source HA switch, etc.) .

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