CABLE POWERING INTO A DISTRIBUTED LOAD

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ABSTRACT

The process of modeling a distributed load cable system is performed. Basic power pack models are developed and tested. A cable network simulation is created using these models to study interactions between components of a distributed load. Steady state testing results show current waveform of a simulated power pack is highly dependent upon location in the network.

Input power disruption is used to study effect of power disturbance in distributed load network. Most significant result is that a small 8mS disruption causes a voltage drop at one node from 43.5VAC to 34.6VAC for a duration of over 50mS. Proves that small transfer times < 10mS can disturb network sufficient to exceed power pack hold-up times.

INTRODUCTION

We felt it was important to more fully understand the characteristics of real cable system powering, which is basically a network of distributed loads. Since it is unrealistic to measure real cable systems (when amplifiers are thousands of feet apart) it is critical to develop accurate models to achieve any meaningful results. The first step in model development is defining the characteristics of a cable plant's components.

INITIAL TESTING

Test Setup for "Actual" Cable Plant

Our initial test setup consisted of five station amplifiers tied together with 875 and 500 cable (still on the spools), powered by a 4 amp 60VAC ferroresonant transformer (Figure 1). Since the cable sheath was uninsulated, we shorted out all of the sheaths with 12 gauge wire to avoid inconsistent measurements.

Test Measurements of Cable Plant

In order to make current measurements we cut away the sheath just before and after each amplifier to expose the center conductor for our clamp-on current probe. The sheath cuts were jumpered to maintain sheath grounding integrity. The RF present on the output of the amplifiers made direct

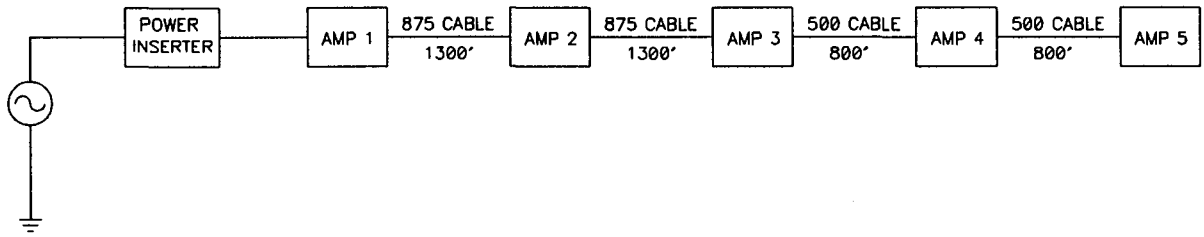

Figure 1 - Initial Test Setup of "Actual" Cable Plant

measurements very difficult. Current was successfully measured using a clamp-on current transformer, which was not affected by the high frequencies. The voltages were measured at the standard test point inside each amplifier.

The clamp-on current transformer was modified with a precision resistor to produce a voltage waveform that accurately represented the current waveform at the test point. This allowed monitoring of the current waveforms throughout the cable plant test setup. These waveforms were recorded on a digital storage oscilloscope and photographed.

Data was gathered on the system's performance in both steady state and disruption conditions. The disruption involved different durations of outages occurring at different phase angles (relative to the incoming AC). The special test equipment used for this is discussed in detail later, along with the testing parameters.

The amplifiers were tested individually by removing them from their housings and plugging them, one at a time, into the first amplifier housing location. This confirmed that all of the amplifiers were behaving in the same way, and provided the data on individual amplifier characteristics.

POWER PACK SIMULATORS

Power Pack Simulation Model

Different methods of modeling the DC power packs found in typical station amplifiers were tried. The final design draws constant power, and is adjustable to match a specific amplifier configuration. A simplified design is shown in Figure 2. The op amp monitors the incoming AC voltage; when the voltage drops, the current draw through the transistor is increased to maintain a constant power draw from the AC line.

It was important to match the Power Pack Simulators (PPSs) performance as closely as possible to the characteristics of the power packs in the amplifiers we measured. The design is based upon a schematic of the input stage of the DC power pack, using the necessary component values to produce the proper current and voltage waveforms. The input impedence is closely matched (at 60Hz) by incorporating series inductance, a diode bridge, and a 1000μF capacitor. The overall performance is matched by the closed loop constant power sink. The current waveform from a typical station amplifier is matched by the waveform of our PPS, shown in Figure 3.

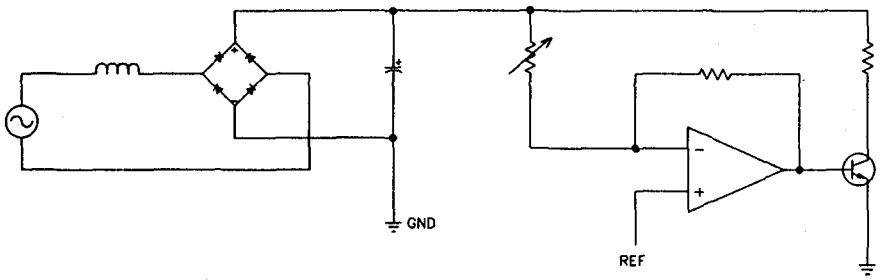

Figure 2
PPS Simplified Schematic

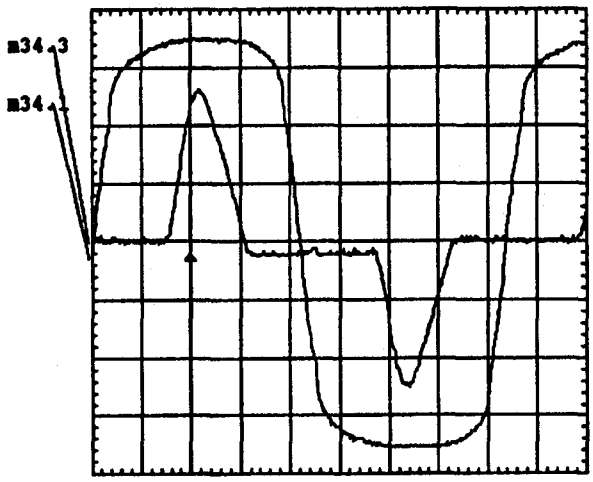

Figure 3 - Single PPS Current Waveform

Source Impedance

A large number of PPSs were built and calibrated using a Variac on the output of a ferro supply with a 0.5Ω series resistor to measure current. Each PPS was tested and set for one of two power levels: 34.6W or 44.2W. The power levels are for two or three output station amplifers, respectively. Each PPS maintains a constant power level (within a few percent) over the range of 60VAC to 40VAC.

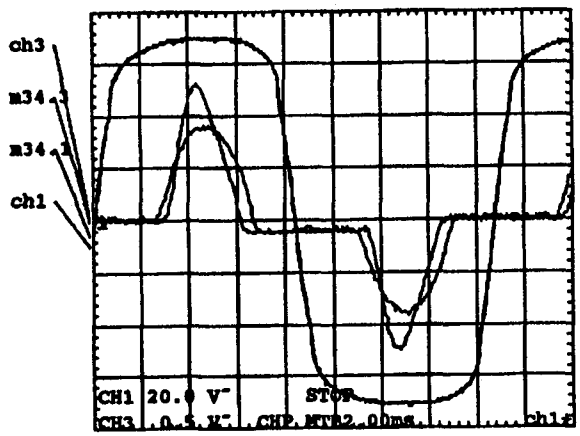

Figure 4 - Source Impedance

The PPSs were then individually tested using different series resistors (for different coax cables) between them and the power supply. A Variac was used to maintain the input voltage to the PPS at 45.5VAC (rms). The current draw (and total power) was reduced when the resistance was increased, even with the same input voltage. The input current waveform changed significantly, as did the total power drawn by the PPS.

The waveform in Figure 4 shows the input voltage and overlays the two current waveforms created with an increase in source impedance from 0.5Ω to 2.6Ω. The current draw is spread out more over time due to the interaction of the series resistance and the large filter capacitor in the PPS. The capacitor cannot draw as much current as quickly with the series resistance, which reduces the current peak. The current draw also occurs earlier due to the fact that the voltage is actually slightly higher at the amplifier during the first part of the waveform. Even though the RMS voltage is the same, when the series resistance is significant, the voltage is initially higher at the PPS since there is no current being drawn at that time. Since the instantaneous voltage level is what causes the capacitor to start drawing current, this allows the capacitor to start drawing current at an earlier time in the waveform.

Another aspect is that the DC voltage across the capacitor is reduced slightly with increased source impedance. This could reduce the potential hold-up time in a power pack by reducing the energy storage level in the DC capacitor.

We believe this phenomenon is present in all switch mode power packs, since it is due to the electrical characteristics of significant source impedance. It is not clear what the measurable effect, if any, on

hold up time might be. The more pronounced effect is the alteration of the current waveform. Of course this is of no consequence in a single amplifier, but when amplifiers are put into a distributed network, then it has an impact on the overall network current waveform, as discussed later.

CABLE PLANT SIMULATION

Network Configuration and Layout

The goal of the layout was to create a model that had some bearing on the real world, but without adding extra complexity which would mask the network response. The concessions to simplicity are powering from the end rather than the middle, and the equal lengths for all similar types of cable runs. The test network layout is shown in Figure 5.

The components being modeled are: two main cable runs of 875 cable with all other cable runs being 500 cable. The total loop resistance for each run of 2000 feet of 875 cable is 1.1Ω, and the total for 1500 feet of 500 cable is 2.58Ω. All of the amplifiers are of the "station" type, with full reverse path capability, using the same switch mode DC power pack. This approach defines the power requirements according to the number of outputs: a two output unit requires 34.6W and the three output requires 44.2W.

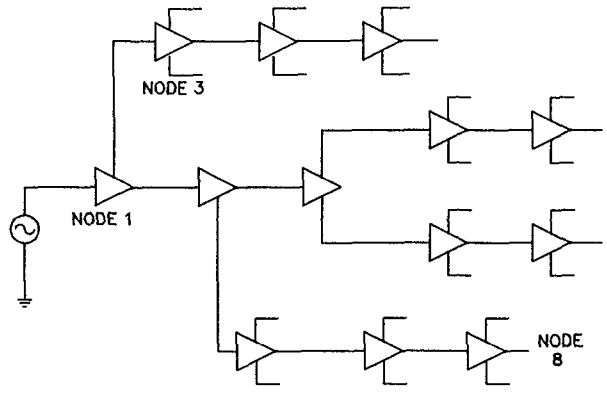

Figure 5 - Test Network Layout

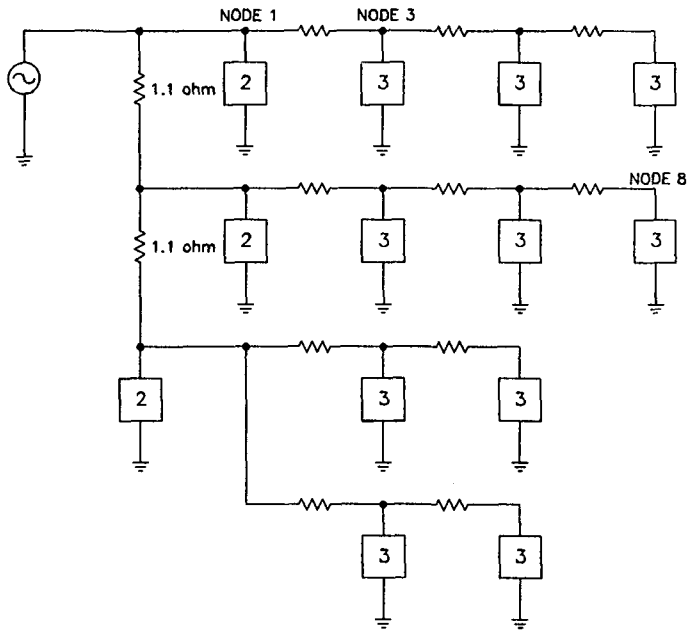

Figure 6 - Test Network Schematic

An electrical engineer looks at this cable network in a different way. Figure 6 shows the same network in a traditional schematic format, which we will use for the rest of this paper. It is assumed that there is no significant impedance (at 60Hz) through the amplifier so the input and output are considered to be the same node. Each PPS (amplifier) is shown as a load interconnected by the resistors which match the loop resistance. Another simplification is that the loop resistance is treated as a single resistance in the power line. All of the amplifiers have the same return potential (ground) to enable accurate voltage and current measurements.

NETWORK WITH STEADY STATE POWERING

The first group of scope displays show the typical waveforms throughout the network during continuous steady state

powering. There are three signals on each display; channel 1 is current into the PPS at that node, channel 2 is the voltage at the PPS node, and channel 3 is the voltage at the power supply that drives the network.

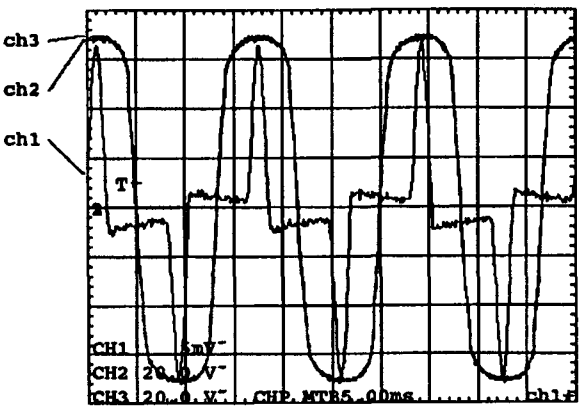

Figure 7 - Node 1, Steady State

Rather than go through all of the data, we will review some of the basic characteristics. Figure 7 shows Node 1. Of course since this node is at the power supply the two voltage waveforms are identical. Note that the current waveform is the same as a single amplfier by itself, shown earlier. The current peaks at 1.7 amps with a rise time of 1mS for a duration of about 3mS. This is characteristic of a capacitive load because the current draw occurs only when the input voltage exceeds the voltage across the capacitor. The fact that the current has a long rise time of 1mS is due to the series inductance in the PPS. The input voltage waveform is quite rounded on top so the highest voltage is in the middle of the waveform, which is when the current is drawn.

The next node, 3, already shows the effect of cable resistance. This is an isolated branch of the network with three PPSs and three cable runs. One of the obvious factors in cable plant interactions is the effect of total current for a branch creating a large voltage drop over the first run of cable. This affects the voltage waveform seen at node 3, as shown by Figure 8. Rather than having the rounded top seen at the power supply, the voltage waveform is much flatter, with a lower peak value (61V). This has the predictable effect of reducing the voltage on the DC capacitor (from 67.0VDC at Node 1 to 59.6VDC) and changing the current waveform. The current draw starts sooner due to the peak input voltage occurring sooner. Other effects include a reduction in peak current, down to 1.3A, and an increase in duration of current being drawn. Note that the rise time remains about the same in this case.

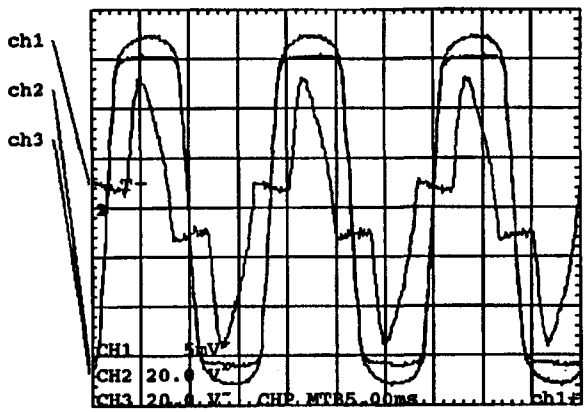

Figure 8 - Node 3, Steady State

The most pronounced effect of cable plant powering is typically seen at the far reaches of a network, where the common condition is being close to "voltage starvation". This is illustrated at three locations in this test network, with the worst being node 8. The voltage at this point is 43.5VAC (rms). In Figure 9 this is seen as a very flat top voltage waveform, with a peak voltage of about 47V.

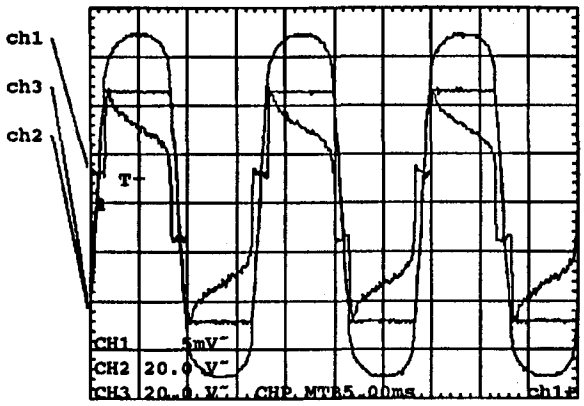

Figure 9 - Node 8, Steady State

The current waveform seen here is very informative. Since the voltage peak occurs very early, the current reaches its peak (of 1.1A) about 1mS after zero crossing (and the rise time is also reduced to about 500μS). The duration of current draw is 7mS, which is the entire time the voltage waveform remains high. It is also interesting that even though the current drops over time, it is still drawing more than 500mA when the voltage turns off.

All of these effects are combined in Figure 10. This display shows the voltage from the power supply and the current going into the test network. In the steady state condition the current draw is concentrated mostly in the center of the voltage wave-

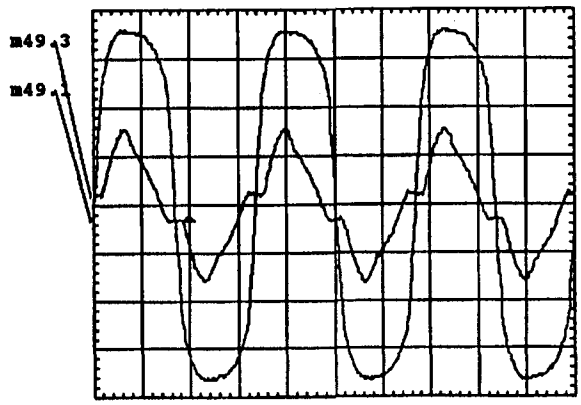

Figure 10 - Network, Steady State

form, but it is also spread out for most of the waveform. It is obvious that there would be a loss of energy to some part of the cable system if the voltage were disrupted almost anywhere in its waveform.

POWER DISRUPTION

Disruption Analysis

There are many different views on transfer time including how it is measured and its degree of importance. An 8mS transfer time has traditionally been viewed as acceptable for Standby power supplies. This is typically justified by pointing to the fact that most amplifiers have a hold-up time on the order of 20-40mS. Even some recent specifications for "UPS" powering of HFC systems only require a 5mS transfer time. This indicates that those writing such specifications feel there is a considerable safety margin in such a time.

It is not our intention to try to mimic how others (ourselves included) perform a transition to standby operation. It is only to introduce a very mild but highly defined disruption into a cable network and analyze the results. In order to generate the most meaningful data in any experiment, it is necessary to eliminate unnecessary complications and variables, and to have a consistent, repeatable, and verifiable test setup. Our goal was to find a way to measure the response of our test network to some type of powering disruption, which would be in some ways relevant to what happens during a non-zero transfer time.

We felt an 8mS disruption (½ of an AC cycle) is actually quite easy on the test network because of this approach: The interruption is not in the output of the power supply to the cable system, as would occur

with a typical transfer relay. In this setup the ferro is still capable of supplying energy to the test network during the disruption, which it does. There is no inverter which eliminates complications of AC detection, response time, and performance characteristics. The same ferro comes back on to supply the test network after the disruption, with the full power of the utility grid as its source.

Special Test Equipment

We developed a special piece of test equipment to allow a disruption of the incoming AC power that feeds our power supply which in turns feeds our test network. The Lectro Controlled Disruption Device (CDD) is a powerful research tool. It monitors the incoming AC voltage waveform and disrupts (turns off) the AC power at a specified phase angle for a specified duration. Phase angle is a way of measuring a periodic sinusoidal signal. The distance from zero crossing to zero crossing (one half of an AC sine wave) is defined as 180 degrees, which takes 8.33mS at 60Hz.

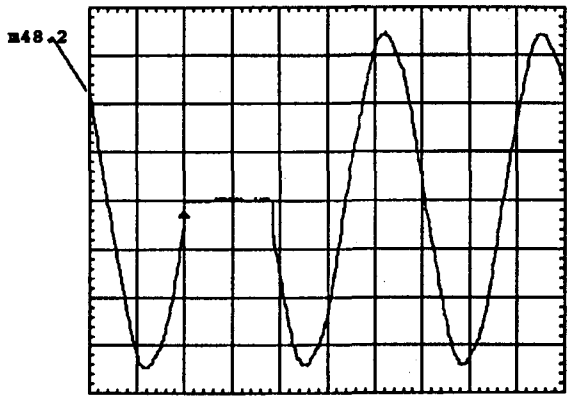

Figure 11 - 0° Disruption, 8mS

The CDD can be adjusted in one degree increments from 0 to ±180 degrees. This allows for very fine adjustment of when

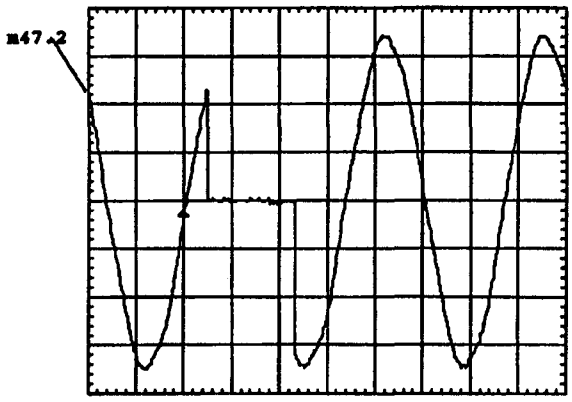

Figure 12 - 45° Disruption, 8mS

the AC signal is removed from the device under test, in this case our power supply. The duration of the outage is also programmable in 1mS increments from 1mS up to 16mS (in its present configuration). This means we can consistantly generate a controlled disruption of the power line in order to see its effect on our test network.

Figures 11, 12, and 13 show the output of the CDD in the three different test conditions. All of these disruptions are for a duration of 8mS; the difference is in the phase angle. The first is at 0 degrees, the second is at 45 degrees, and the third is at 90 degrees.

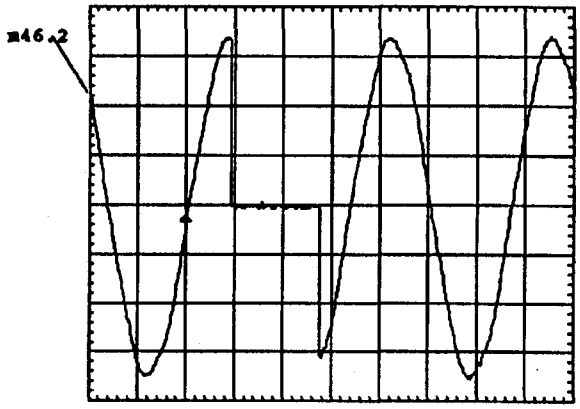

Figure 13 - 90° Disruption, 8mS

NETWORK WITH POWERING DISRUPTION

Test Parameters and Setup

Three phase angles: 0°, 45°, and 90° were used as the test parameters for the disruption testing. This defines when the disruption starts relative to the incoming utility AC voltage waveform. All of the disruptions were set for a duration of 8mS, as described earlier. As a reminder, the 0° disruption cuts off a full half cycle, the 90° disruption shuts off from one positive peak to the next negative peak, and the 45° disruption cuts off ¾ of one half cycle and the first ¼ of the next.

The displays consist of channel 1 as the current waveform at the node under test, channel 2 as the output voltage from the power supply, and channel 3 as the voltage at the node under test. All of the waveforms are AC and centered on the display. A small triangle, located two divisions in from the left, indicates the trigger signal input from our CDD. Note that this trigger fires on the last zero crossing prior to the disruption (it is simultaneous with the disruption at 0°).

General Observations

There are some common traits seen in all of the following displays, Figures 14 through 22. Several are inherent to a ferro-resonant transformer, while others relate to the PPS and the network itself.

First is the fact that even with a positive power disruption, there is still voltage being supplied to the load by the ferro. As shown by the displays in Figure 14, there is also some current being supplied at this time. Note that the scale for current in this display is 10A per division. Power is being delivered to the load with no power coming in. This is a clear example of the energy storage capabilities of a ferro transformer. Of course there is a price to pay for this "free" energy, as discussed below.

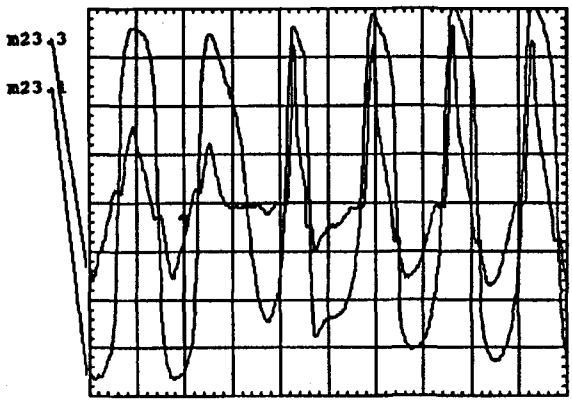

Figure 14 - Network, 90° Disruption

The price is that the ferro must recover its energy when the input power is restored in order to become a stable regulated voltage source. One impact is a voltage overshoot during the first half cycle after return of power from a disruption. In this case this is a big benefit to the test network because a voltage spike provides assistance to all of the PPSs in recovering the energy they lost during the disruption (note several current spikes over 30A in Figure 14). This voltage overshoot is common in closed loop control systems (which is what the secondary winding of a ferro is). Along with the spike there is a frequency distortion during the first cycle, which is another ferro characteristic during energy loss. It is important to remember that these ferro actions are typical of a stand-alone ferro under these disruption conditions; they do not occur in a properly designed zero transfer time power supply.

Another common trait of the test network is the ability of the PPS to store excess energy. This is seen during the ferro

overshoot when the current spikes throughout the test network. Some of the PPSs can go several cycles before needing to draw current again.

The last general observation is the confirmation that interactions exist in the test network. This is seen in the different voltage and current responses at the different nodes of the network during a specific disturbance. It is also evident from the significantly different reactions that the same nodes have to each different disruption. The cause and effect relationships are highly interdependent, making predictions difficult. As one node within the network does not pull current because it stored enough on the previous cycle, it means the voltage drop along its feeder cable is reduced by that amount, which potentially raises the input voltage for the following nodes. However, if a node pulls more current because its input voltage was raised, it drops the voltage for the following nodes. All of these interactions are happening at the same time, even within a particular half cycle. That is why detailed measurements of a test network under known conditions provide the best insight into this interaction.

Current Waveform Analysis, 0° Phase

At node 1, both power supply and input voltages are the same since there is no series resistance element (Figure 15). The power supply voltage drops in the first half cycle (during the outage) from its normal peak of 69V to a peak of 54V. The next half cycle peak is off scale (above 80V peak) since the power is now restored to the ferro. The ferro is still recovering during the next half cycle with a peak of 64V, with some distortion.

The current waveform during the first

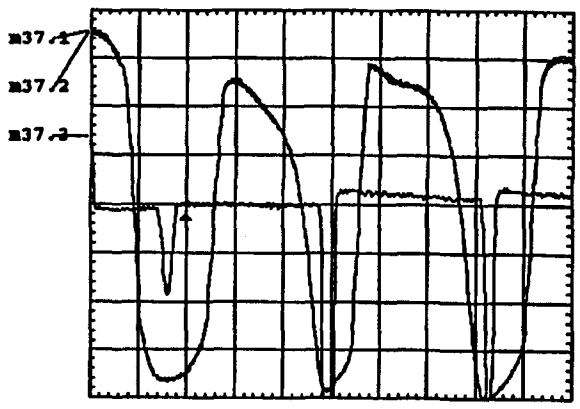

Figure 15 - Node 1, 0°

half cycle (when the voltage drops) shows no current draw, followed by a sharp current spike (along with the voltage spike) during the next half cycle. After this point (not shown in figure) the PPS does not draw any current for over 60mS (7½ cycles) even though the node voltage is clearly back to normal within two cycles.

At node 3 (Figure 16) the input voltage during the outage cycle is identical to the power supply voltage. This is because virtually none of the PPS devices draw any current during this time so there is no voltage drop, even out to the end of this cable run. The next half cycle (as power is re-

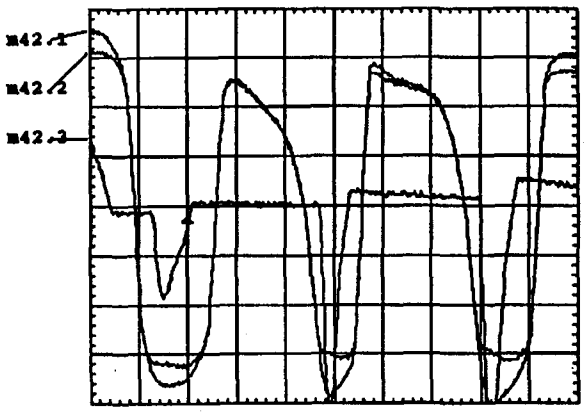

Figure 16 - Node 3, 0°

stored) shows that while the power supply voltage peaked at over 80V, the input voltage at this node only peaked at 69V, which is not much above its nominal peak of 64V. As many of the PPS devices close to the power supply benefit from the voltage by pulling more current, the price is a significant increase in the voltage drops across the network cables. The next half cycle shows no current draw, followed by a slightly larger than normal draw for the next. This erratic pattern repeats for several cycles before damping back to its steady state condition.

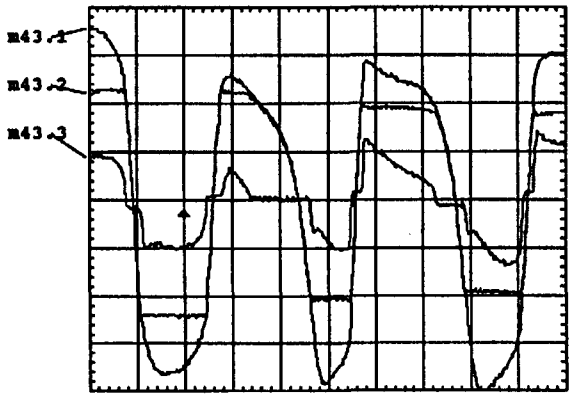

Figure 17 - Node 8, 0°

Node 8 (Figure 17) displays a completely different current response than the previous two nodes, primarily due to its location (see Figure 6). First is the fact that it draws current during the first 2mS of the outage. Even though the ferro's voltage is dropping, the lack of currrent draw else where in the network allows node 8's input voltage to be almost normal for a few mS. The next half cycle (when power is restored) is very telling: even though the ferro's voltage goes above 80V, the input voltage at 8 drops to less than 42V. Current is still being drawn, though only during the last few mS of the cycle, as its input voltage slightly increases. The input voltage is still dropping (around 38V peak) during the third half cycle while current spikes to over 1.5 amps. Unlike nodes A1 and A3, which pulled peak currents for one or two half cycles then drew very little, node A8 is pulling high peak currents for several cycles after the disruption and never draws less than its nominal peak.

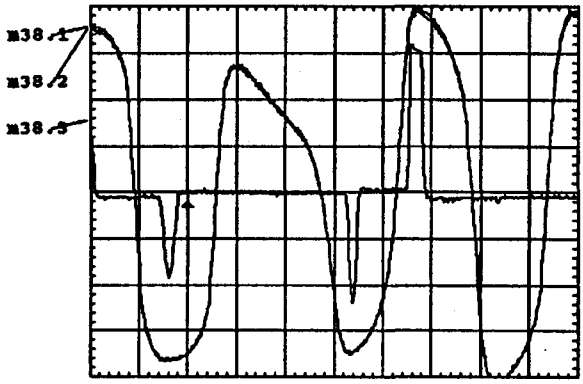

Figure 18 - Node 1, 45°

Current Waveform Analysis, 45° Phase

The differences between the nodes 1, 3, and 8 were discussed above, so only those conditions that are different due to the phase angle will be covered. Node 1 (Figure 18) shows a very similar response, except under this condition the ferro generates two voltage spikes over 80V peak instead of one. This leads to two current spikes, then the typical

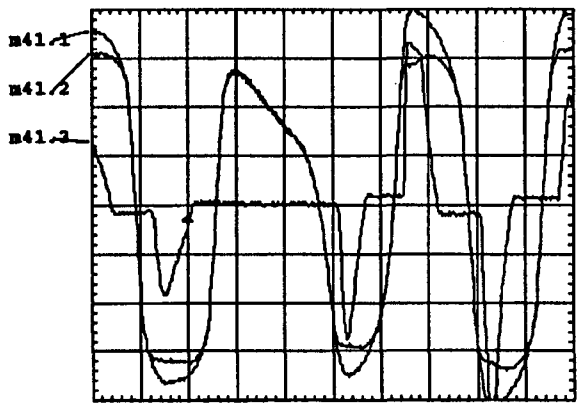

Figure 19 - Node 3, 45°

multicycle duration of no current. Node 3 (Figure 19) shows a similar pattern as before with the modification of the second voltage spike.

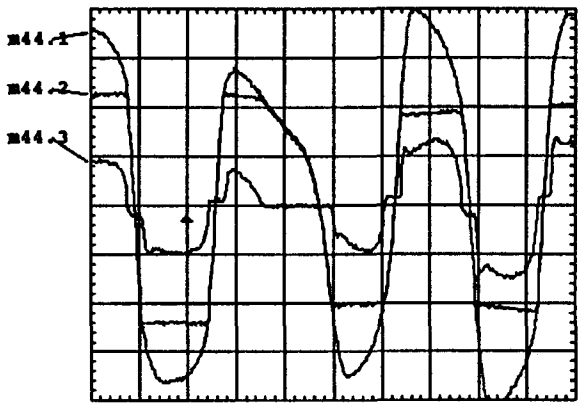

Figure 20 - Node 8, 45°

Node 8 (Figure 20) again pulls current during every half cycle, but this time it recovers back to steady state in about three cycles. It is interesting that node 8 recovers quicker at 45° than at 0° or 90°. This is probably due to the interactions of all of the plant simulation components finding a balance under this set of conditions.

Current Waveform Analysis, 90° Phase

The node 1 display (Figure 21) shows the impact of this disruption on the power

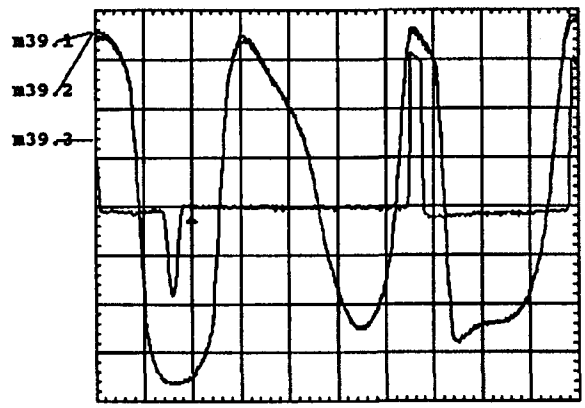

Figure 21 - Node 1, 90°

supply waveform. It reaches its normal peak voltage, then drops off quickly. The next

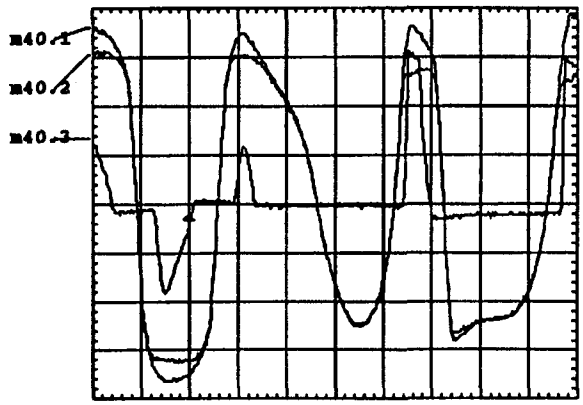

Figure 22 - Node 3, 90°

half cycle is much lower with only a 46V peak. Energy returns in the third half cycle with the voltage peaking around 80V. Node 1 shows two complete half cycles of no current, followed by a current pulse corresponding to the return voltage pulse.

Node 3 (Figure 22) demonstrates how its lower nominal voltage masks the effect of the power supply's voltage drop as it pulls a significant portion of its normal amount of

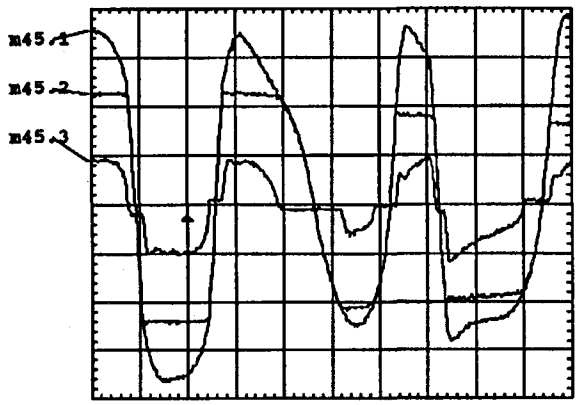

Figure 23 - Node 8, 90°

current. Again the effect of current flow throughout the network is seen in the differences (or lack thereof) between the input voltage and the voltage at the input of 3.

Node 8 (Figure 23) pulls almost all of its current during the first half cycle, and even manages a small amount in the second half cycle. This is followed by many different patterns of current waveforms. Node 8 is attempting to pull current from anywhere it can.

Voltage Waveform Analysis, 90° Phase

It turns out that the most informative view of the effect of an 8mS disruption at 90° is the voltage waveform. Figure 24 shows the input voltage at node 8. This

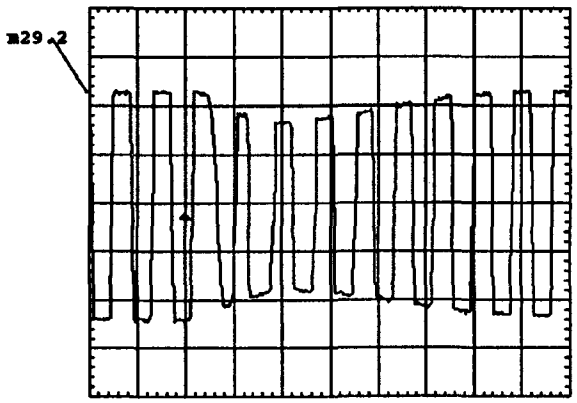

Figure 24 - Voltage Drop, Node 8, 90°

clearly shows a drop in voltage over several full cycles. More specifically, it shows a drop in peak (nominal) voltage from 47V to a minimum of 35V. What is surprising is that it also shows a drop from 47V to below 37.5V for more than 50mS. This can be related to an amplifier normally running at 43.5V rms that goes down to 34.6V rms for at least 50mS, all from a single, simple disturbance of only 8mS.

ZTT POWERING OF NETWORK WITH DISTURBANCE

A Lectro ZTT was installed to power the test network. The CDD connected to the AC input of the ZTT to disrupt power as in the previous test setup. The resultant waveforms, shown in Figure 25, are for node 8 with an 8mS disruption at 90°. The voltage at the power supply shows a slight drop, but the voltage at node 8 remains constant, except for the slight rise in peak voltage (2V) during the second half cycle. There is no voltage loss at node 8 with the ZTT, as was previously shown in Figure 24.

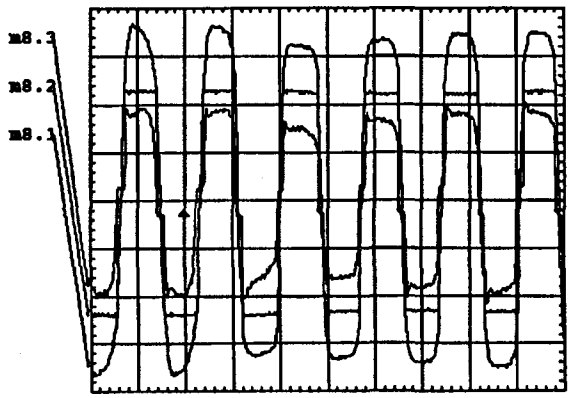

Figure 25 - ZTT Power, Node 8, 90°

The current at node 8 shows a slight rise in the second half cycle which matches with the voltage rise. For the next few cycles the current drops slightly before returning to normal. This waveform is nearly identical to the steady state waveform seen in Figure 9 (except for different time base).

RESULTS

This is by no means an exhaustive review of the impact of disruptions, resulting disturbances, transfer times, etc. It is only the tip of the iceburg in developing a solid understanding of distributed load powering.

The most significant result of this limited testing program is the significant voltage drop for such a long period of time from such a short disruption. In this setup, the worst condition found (so far) is at node 8 with a disruption of 112°.

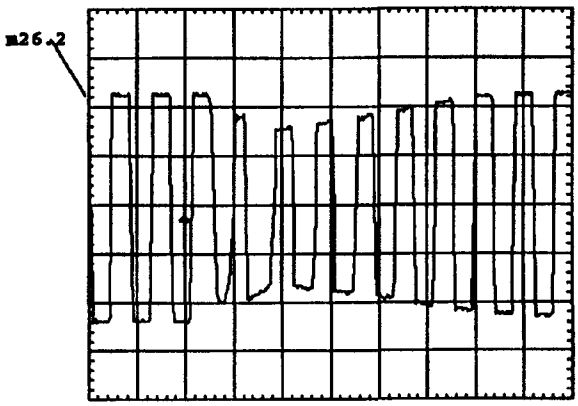

Figure 26 - Node 8: 112°, 8mS Disruption
Voltage drop: 43.5VAC to 30.1VAC
Duration: 69.6mS

The depth and duration of the voltage drop at node 8 is due to the characteristic interaction seen in a distributed load. The series resistances that represent the cables of a real system are the elements that modify the voltages throughout the cable plant during any disturbance in powering, no matter what the source.

CONCLUSIONS

It is obvious that transfer time, or anything that disturbs the power source output, has significant effects. It is clear that trying to claim transfer time is acceptable because it is smaller than an amplifier's hold-up time is wrong; there is no direct relationship.

Some large MSOs are starting to require low voltage limits on amplifiers, where the DC power pack goes off line if the AC input voltage drops. It is realistic to believe that an amplifier with this feature would probably shut itself down and lose its output if located at node 8 in this test network.

Considering the direction of the industry towards higher reliability and the desire to provide lifeline telephony services, the powering of any cable plant should include provisions to eliminate any source of power disturbances.

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