

## THE ADVANTAGES OF BASEBAND VIDEO SYNCHRONIZATION

Stanley R. Moote, P.Eng., BASc

Leitch Video Limited

As television cable systems grow more complex, new problems arise and some become more prominent. One significant problem is co-channel interference. By aligning the synchronizing intervals of all channels, the subjective impairment due to crosstalk can be reduced. This can be accomplished by baseband processing with digital frame synchronizers. A digital frame synchronizer stores the incoming baseband signal and outputs it with the synchronizing interval aligned to that of a reference baseband signal. This storage and retrieval process takes place in the digital domain.

There are other benefits realized with the use of frame synchronizers. Title keying and channel switching techniques are simplified and improved. Since the synchronizing interval is replaced, improvements in post production editing and mixing are achieved. In addition, corrections can be made to the contrast, color and black level.

### Co-channel Interference

Within cable systems, co-channel interference degrades signal quality as more channels are added to the system. One of the many factors which adds to these signal degradations is inter-modulation distortion (IMD). IMD is caused when a signal with two or more frequency components passes through a non-linear device. The distortion is magnified as the input signal level increases. This can be readily seen on a spectrum analyzer.

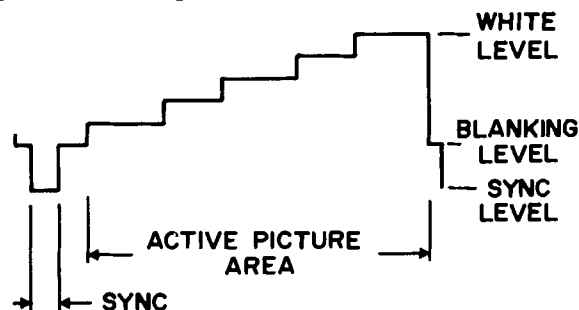


Figure 1.

Figure 1 shows one single horizontal scan line. This signal contains synchronizing and active picture information. The active picture starts with black, stepping towards white. Note that the sync area is below black.

NTSC signals are modulated using the vestigial sideband method. The RF envelope is maximum during sync (fig. 2). Maximum crosstalk occurs, therefore, during the sync interval. There are two benefits for having maximum energy transmitted during sync: (1) The television receiver located a great distance from the transmitter will maintain lock even when the picture may be very noisy and difficult to view. This was a very important feature in North America prior to the advent of cable distribution. (2) It provides a method of readily measuring the peak power output of the transmitter.

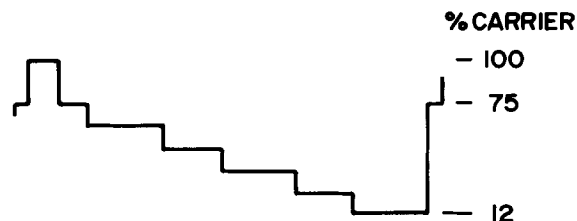


Figure 2.

When two or more non-synchronous TV channels are fed into a non-linear device, such as a line amplifier, the sync periods and hence the crosstalk will move with respect to each other. By matching all sync periods in the time domain, there will be less visible crosstalk in the active picture area. Observing the signal behaviour on a spectrum analyzer will show an apparent crosstalk increase unless the Z-axis of the analyzer is modulated with blanking. This process of sync alignment (sync lock) must be done with digital frame synchronizers, one for each program channel.

### Definition of Baseband Video Synchronizer

A synchronizer matches the timing of a program video signal to that of a master reference signal. This re-timing is done with digital processing techniques and makes use of the segmented nature of the video signal. In the synchronizing process, baseband video may be compared to a clock:

Color sub-carrier is the second hand  
Horizontal scan is the minute hand  
Vertical scan is the hour hand

The plant, where these signals are to be processed, needs a master reference clock which is obtained from the plant sync pulse generator. The program signal must be timed to this reference clock. Suppose the reference clock hands are pointing at 12:00:00 while the program clock hands are at 4:30:00. This means the program signal is ahead of the reference signal. In order to match the program signal with the reference, a delay of four hours and thirty minutes is needed. The numbers used here are for demonstration purposes only, since each vertical scan takes 17 milliseconds. The required delay can be easily obtained with digital techniques, whereas an analog solution is costly and impractical.

### Variable Digital Delay

A variable digital delay device converts an analog signal into digital words. These words are stored in memory and later recalled to match the reference signal. The length of obtainable delay is a function of the size of the available memory.

To give another example, let us assume that the program signal is at 11:58:00 and the reference is at 12:00:00. Since the program signal cannot be advanced by two minutes, it must be delayed by eleven hours and fifty-eight minutes. To add more complexity to the problem, let us further assume that the program signal clock is moving faster than the reference clock. This means that at some point, when the reference clock is at 12:00:00, the program clock will be at 12:01:00. If we were to continue adding delay to match the two clocks, we would eventually require an infinite amount of delay. In the example just given, it would be simpler to drop twelve hours and only one minute of delay would be needed. This keeps the digital delay required at any given time to a minimum.

If the program clock is slower than the reference, adding twelve hours is necessary. Since the program signal is stored in memory, the last twelve hours can be repeated to match the two signals.

I have shown in the foregoing analogy that a video synchronizer uses digital memory to delay and thus align two baseband video signals. I will now briefly describe the Leitch DFP-3000N Digital Frame Processor. This unit contains a full four-field digital memory. Along with providing the necessary delay to synchronize baseband video signals, it also allows adjustment of various signal parameters. This is done on the unit's front panel, using a unique, microprocessor-controlled operator interface.

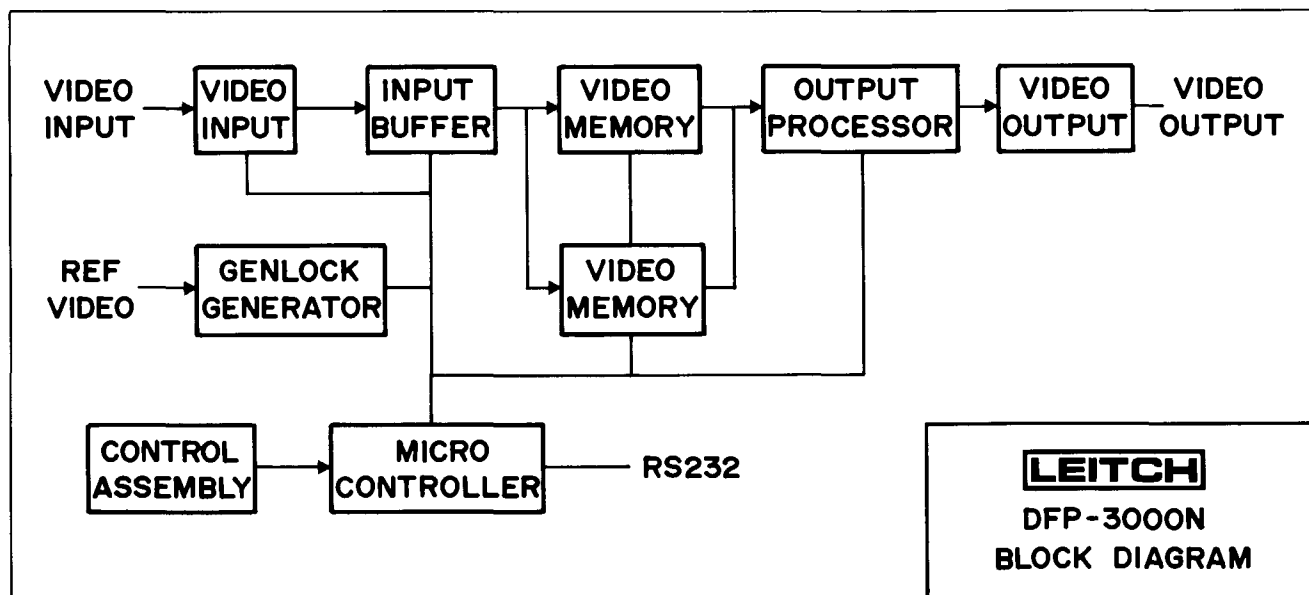


Figure 3.

### Video Synchronizer Hardware

The block diagram of a Digital Frame Processor (figure 3) shows two signal inputs and a single output. The program video is fed into a differential input amplifier and then passed through a variable gain stage as well as a chroma gain stage. This signal is DC restored, passed to a sync stripper and also provides an input to an analog to digital converter (ADC). The ADC converts its analog input to an eight-bit word at a 14.3 MHz rate (four times the color subcarrier frequency). Both, video level and chroma gain stages, as well as the DC restoration stage (set-up) are digitally controlled by a microcomputer. The ADC has a fixed dynamic range, and in order to preserve optimum signal-to-noise ratio throughout the system, the variable processing functions are done in the analog domain and before the ADC (quantizing noise). This sampled data, as well as stripped sync, is passed to an input processor board.

The purpose of the input processor board is to convert the program signal data rate to that of the reference. Three first-in-first-out (FIFO) memories are used here and provide more than enough buffer memory in order to allow the synchronization of a single video line. One point of interest here: to save on the amount of memory needed, only the active portion of the video is stored. The sync and burst areas are re-inserted at the output of the system.

Once the program line of video is aligned horizontally with the reference signal, the video must be aligned at the frame rate. To achieve this, 768 kilobytes of memory is used. This memory is split between two boards. Each board has enough memory to store two fields of video. A new type of dynamic random access memory (RAM) is used in the DFP-3000N with a configuration of 64K by one bit and a 256-bit internal shift register. Since there are 768 digital samples taken across each video line, three memory chips are cascaded to provide a 768-bit shift register. This shift register configuration requires only one write and read cycle per video line. Since these cycles require less than 1 microsecond, more than 60 microseconds are available for the microcomputer to access these video RAMs.

The system phase-locks (genlocks) to a reference input signal on the genlock generator board. This genlock generator passes control signals to a microcomputer

controller and a blanking processor board. The blanking processor generates most of the signals needed to control the video memory.

The microcomputer receives information from the input and output processors to decide how much synchronization delay is necessary and, in turn, controls the two memory boards. The processor also reads the front panel control assembly as well as the remote panel to provide the necessary processing data to the input circuitry. The DFP-3000N was designed to sense both loss and change in the program signal. These sensors are noise immune and are fed to the microcomputer. The microcomputer correlates the sensed data and adaptively controls the memory. One example of this is how the system will control a non-synchronous switch of program video. The system may freeze the last good field of information until the input stage is re-locked to mask the locking process. It is important to note here that the system will always output stable sync and burst.

An RS-232C port on the microcomputer allows the user direct access to the video memory. Via this port the user may freeze a field or frame of video. This data can then be transferred to a host computer. After manipulation in the computer, the changed data are sent back to the Digital Frame Processor. All processing functions are available via this port. The plant that has several Digital Frame Processors may connect all of the RS-232C ports together through a computer. This allows control of each Digital Frame Processor from a single control point.

A variety of video test signals are also present within the microcomputer's firmware. These are used for diagnostics and calibration.

The synchronized video data from the memory is routed to the blanking processor. Here it is digitally filtered to maintain the correct color. With four fields of memory, the color is always correct without any horizontal shifts. The color is corrected only under field-freeze conditions. Sync and burst signals are now inserted into the data stream. This data is now passed to a digital-to-analog converter (DAC). The output of the DAC is again filtered, amplified and then appears at the 75 Ohm output BNC connector.

### Other Benefits

Having described the hardware of the DFP-3000N Digital Frame Processor, I will now briefly discuss further benefits of synchronized syncs within a cable system. When all signal feeds are horizontally and vertically aligned, post production work, such as channel switching or insertion of local program material, becomes glitch-free. Title keying or news flashes can also be added on all channels at once with one generator, or by using the RS-232C port of the DFP-3000N.

The Digital Frame Processor doubles as a processing amplifier. Uniform picture quality on all channels is possible since each Digital Frame Processor allows corrections for color, contrast and brightness. Post production work is improved because the off-air sync and color burst is replaced with stable sync and burst.

A strong local channel is likely to plague a cable system. Its signal manages to interfere with its cable counterpart. Provided that the local station always maintains stable sync, the cable system could use the local channel as a locking reference to reduce blanking bar interference.

Phase-locked cable systems lock only the main carrier of all cable channels to a single reference. The color subcarriers cannot be phase-locked together unless the system is sync-locked. By using DFP-3000N Digital Frame Processors on all channels, not only will all the syncs be aligned, but all of the color subcarriers will also be synchronous. This again provides visible picture improvement.

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The author wishes to thank Mr. George Adolph and Mr. Don Jackson for their help in the preparation of this paper.