BANDWIDTH-EFFICIENT, HIGH-SPEED MODEMS FOR CABLE SYSTEMS

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ABSTRACT

Because of recent interest in cable systems for data transmission as an alternative to use of telephone company leased lines, Scientific-Atlanta is introducing the 6402 High-Speed Modem which is capable of transmitting and receiving data at standard telephone system rates of 1.544 Mbps (T1) or 6.312 Mbps (T2). Two features of the 6402 are especially useful for operation on cable systems: high bandwidth efficiency and frequency agility.

The 6402 design is composed of two major parts: the RF section and the baseband processor. The RF section provides modulation, demodulation, frequency translation, and frequency synthesis. The baseband processor recovers both the carrier frequency and the data rate clock from the demodulated baseband signal provided by the RF section using digital processing.

The basic technique used in the 6402 is Quadrature-Amplitude-Shift-Keying (QASK). This method of modulation allows frequency spacing of 750 KHz for T1 channels and 3 MHz for T2 channels with a bit error rate of less than 10^{-9}.

INTRODUCTION

The advent of well-designed coaxial cable networks covering large, metropolitan or suburban areas has led to a high degree of interest in the use of these networks for data communications. Because of the large available bandwidth, in excess of 400 MHz coaxial systems represent an excellent medium for digital communications. With the requirement for commercial systems of C/N $\geq$ 36dB, i.e. C/No $\geq$ 102dB-Hz, and the ability for good designs to exceed this by as much as 9dB[1], complex, wideband digital modulation formats can be supported. Because commercial systems are designed to distribute primarily video modulation formats, the transmission system must be maintained in a highly linear mode, thus modulation schemes which may suffer when confronted with the nonlinearities inherent in satellite communications, for example, may be employed with relative inpunity on the coaxial medium. All of the above factors became apparent resulting in the current industry drive to develop data communications capability on existing, planned and future coaxial systems.

In September 1981, Scientific-Atlanta installed a demonstaration data link in order to show the feasibility of providing wideband data services via coaxial cable. This initial installation provided local distribution of 96 voice channels between ISACOM, Inc., operating Satellite Business Systems (SBS) digital earth terminals in Atlanta and Houston, and one of their customers, National Data Corporation (NDC). This link was established with a dedicated cable pair (for redundancy) installed and maintained by South Media, Inc. The link provided NDC with voice and data services between their offices in Atlanta and Houston. Two crucial features of data communications over coaxial systems were demonstrated. The first was that transmission performance was limited only be terminal equipment, the cable medium performed transparently. The second feature involved communication economies. Coaxial cable was unrivalled when cost was a consideration.

Since the installation of this first link a third fundamental principle was uncovered. While the cable offers unparalled cost and performance for high speed data communications its bandwidth must be treated as a highly prized commodity. The installation of wideband full duplex links at T1 (1.544Mbps) and T2 (6.312Mbps) rates employing modulation techniques with moderate bandwidth

efficiency, e.g. 0.5 bits/Hz, would only permit 19 T1 links or 4 T2 links on a mid-split coaxial cable network as shown in Figure 1. Therefore, the capacity of the network is greatly enhanced when more efficient modulation techniques are applied. At 2.0 bits/Hz, 76 T1 links or 38 T2 links can be supported. Application of current digital communications technology is essential in order to effect more efficient utilization of the available bandwidth. It was therefore determined that an approach was necessary which would maximize spectral efficiency without driving manufacturing costs to prohibitive levels. A technique satisfying these requirements has been developed and is the subject of the remainder of the paper.

SYSTEM DESIGN

In order to meet the necessary bandwidth efficiency requirements for high speed data transmission, the selection of the modulation format was essential. While spectral efficiences of 0.5b/Hz - 1.0b/Hz are readily achievable it was determined that 2b/Hz could be realized without undue additional manufacturing cost. This was possible due to the ease of implementation of the selected QASK-16 signal constellation, in both the modulation and demodulation processes. QASK-16 is a special case of the Mary Amplitude-Phase-Shift-Keyed (MAPSK) family of signal sets which provide enhanced bandwidth efficiency through efficient signal packing at the expense of bit error probability, P_b, in the noisy enviornment. However, since coaxial systems provide high signal-to-noise ratios, these complex modulation formats are applicable.

A performance goal of $P_e < 10^{-9}$ was established for the data link thereby constraining the modulation complexity due to the fixed limit of $C/N_o \geq$ 102dB-Hz. A large body of literature exists on studies and hardware implementations covering many of the MAPSK signal sets [2 - 11]. After an evaluation of the myriad possibilities it was determined that QASK-16 offered the best compromise of spectral efficiency, P_b, and cost of implementation. The average symbol signal-to-noise ratio, $R_d \triangleq ST/N_o$, is easily found to be $R_d \geq$ 46dB for a coaxial system operating at marginal performance levels or better and a T1 bit rate (QASK-16 transmits four bits per symbol). However, data signals cannot be permitted to operate at power levels in excess of the video signals with which they must co-exist. Therefore, it was determined that the power of each digitally modulated carrier be 15dB below video levels for T1 and 9dB for T2. This results in a total channel power (6 MHz channels) 6dB below a corresponding video channel when the channel is fully packed with T1 or T2 data carriers at .75 MHz and 3 MHz spacings respectively. This requirement reduced the worst case to $R_d >$ 31dB for both rates. In order to achieve a symbol error probability, Ps, of 10^{-9}, Rd > 26dB is a lower bound when implementation losses are included. Thus, 5dB of system margin exists for the QASK-16 modulation scheme.

The QASK modulation format selected from the family of MAPSK signal sets does not represent the optimum signal set, however it has been shown to be degraded from the optimum by only tenths of a dB [3, 5]. This penalty is insignificant when faced with the complexities of implementation of the alternatives. Through the combination of several decision directed or decision feedback techniques, all of the functions necessary for demodulation of the QASK signal set will be shown to be readily implemented.

System Model

The basic models for the QASK communication link are shown in Figure 2. The incoming data stream, d(t) is scrambled to insure adequate symbol transitions, then taken four bits at a time and differentially encoded [12], then filtered to provide minimum bandwidth and inter-symbol interference (ISI) and impressed on quadrature carriers. The transmitted signal s(t), an M-ary quadrature-amplitude-shift-keyed (QASK-M) signal with a symbol interval of T-seconds, can be represented mathmatically as

$$S(t) = \sqrt{2}[m_i'(t)\cos w_o t + m_q'(t)\sin w_o t] \quad (1)$$

where $m_i'(t)$ and $m_q'(t)$ are scrambled, encoded and filtered pulse trains. These quadrature pulse trains take on equally likely values $j\delta$ with $j = \pm 1, \pm 3, \ldots, \pm (K-1)$ in each channel. Thus for $K=4$, the case of interest here, $m_i'(t)$ and $m_q'(t)$ are the filtered versions of amplitude shift-keyed (ASK) inputs with equally likely values of $\pm\delta$, $\pm 3\delta$, resulting in the QASK-16 signal set with two amplitudes and two phases in each quadrature channel. The average signal power of the transmitted signal set is

$$= 2/3(K^2 - 1)\delta^2. \quad (2)$$

This transmitter model is depicted in Figure 2a.

The channel shown in Figure 2b is assumed to be an additive white Gaussian

noise (AWGN) channel where the noise n(t) has a two-sided spectral density $N_o/2$ W/Hz. In addition the channel adds a random phase shift to the signal s(t) such that the received signal is of the form,

$$x(t) = s[t,\theta(t)] + n(t) + J(t)$$
$$= \sqrt{2}\{m_i'(t)\cos[w_o t + \theta(t)] + m_q'(t)\sin[w_o t + \theta(t)] + n(t) + J(t)\} \quad (3)$$

where $\theta(t) \triangleq \theta_o + \Omega_\theta t$, with θ a uniformly distributed phase shift and Ω_θ the frequency shift from its nominal value of w_o. The additional signal J(t) represents additive interence signals which though present in practice are assumed negligible in the discussion to follow.

The receiver model is shown in Figure 2c where the input signal, X(t) is multipled by a locally generated quadrature reference,

$$r(t) = \sqrt{2}\cos[w_o t + \hat{\theta}(t)] \quad (4)$$

where $\hat{\theta}(t)$ is the local estimate of $\theta(t)$. Because the case of interest here is that of very high R_d, the noise will be neglected in further discussions, the case of low-to-moderate R_d is treated adequately in the references.

The quadrature signals multipled by the reference and again Nyquist filtered are represented as

$$z_i(t) = m_i'(t)\cos\phi(t) + m_q'(t)\sin\phi(t)$$
$$z_q(t) = -m_i(t)\sin\phi(+) + m_q'(t)\cos\phi(t)$$

where $\phi(t) \triangleq \theta(t) - \hat{\theta}(t)$ is the carrier recovery loop phase error. The baseband signals, $z_i(t)$ and $z_q(t)$ are then quantized in an analog-to-digital converter, and processed in order to recover the carrier phase process, symbol synchronization, detect the transmitted symbols, control the gain and detect lock. The algorithms necessary to provide these functions are implemented in a digital processor the details of which are left to a subsequent section. The carrier recovery algorithm employs a decision-feedback technique analyzed by Simon and Smith [13]. The symbol synchronization algorithm is a generalized data transition tracking loop, similar in concept to that analyzed by Simon [14-15]. The AGC algorithm is a decision-directed technique as analyzed by Weber [16], with the lock detection algorithm employing the AGC error signal as its decision criterion. The channel encoding is essentially differential encodng and is necessary in order to remove the quadrant ambiquity in the received symbols. The filtering for bandwidth efficiency, or Nyquist filtering, compresses the transmitted spectrum to achieve the 2 bits/Hz spectral efficiency while minimizing ISI. The filter is partitioned between the transmitter and receiver in order to minimize adjacent channel spillover and adjacent channel interference respectively.

The modem developed for the mid-split cable system is designated the 6402 High Speed Modem. A functional block diagram of the 6402 is given in Figure 3. Each of the elements in the diagram are described in more detail in later paragraphs. The salient features are the frequency agility provided by transmit and receive synthesizers, low spurious emissions allowing for reliable coaxial network operation, and a high performance baseband detection technique resulting in $P_b \leq 10^{-9}$.

RF SECTION

The RF Processor is comprised of the transmit and receive IF assemblies as well as the transmit power amplifiers, receive amplifiers and the synthesized local oscillators (LO's). A mid-split diplexer is used to interface the transmit and receive assemblies to the cable. While filtering is performed in both the transmitter and receiver of the 6402 none of these filters affects the modulated signal. The spectral efficiency is achieved through baseband filtering in the baseband processor. The design philosophy adopted for the RF Processor was to employ standard components in a way such that highly reliable RF signal processing was possible without generating interference which would affect the performance of other signals on the coaxial network.

Transmitter

The transmitter is composed of several elements: The quadrature modulator, synthesized transmit LO, and power amplifiers. The modulator employs a 145 MHz TCXO as an IF, which is then modulated by the in-phase and quadrature ASK symbols, $m_i'(t)$ and $m_q'(t)$ as described previously. These quadrature signals are summed resulting in the QASK-16 signal. This signal is filtered with a broad IF filter, amplified, and then translated to the transmit frequency by the transmit LO which results in 0.75 MHz channel spacing across the reverse channel, 5-102 MHz. Filtering in the transmitter amplifier stages rejects the TX LO such that the worst case spurious output is -60dBc.

Receiver

The receiver assemblies are composed

of broadband amplifiers, the synthesized receive LO, and the quadrature demodulator. In order to prevent leakage of the RX LO onto the cable, each receiver broadband amplifier is preceded by a compensating attenuation, such that the net gain is essentially 0dB. This inserts the necessary isolation to keep the spurious levels due to the RX LO at $\leq$ -60dBc. The RX LO then provides the necessary conversion frequency, with .75 MHz resolution, to translate the receive channel to the 150 MHz receive IF. In the IF, the signal is amplified and filtered with a broad channel filter with 10 MHz bandwidth to reject undesired channels. A PIN diode attenuator is employed in the receive IF for processor control of the input levels. This signal is then applied to two mixers using the reconstructed carrier references as supplied by the Baseband Processor to demodulate the incoming signals to baseband. At this point the quadrature baseband signals are applied to the Baseband Processor inputs for digitizing.

BASEBAND PROCESSOR

Technology

With careful use of a few state-of-the-art components, it was possible to build most of the baseband processor with standard MSI-TTL technology rather than more expensive ECL. An example of a critical section is the numerically controlled oscillator. The 5 MHz NCO requires the fastest TTl PROM and TTL registers commercially available.

Algorithms

The major functions of the baseband processor are shown in the block diagram of Figure 4. The carrier synchronization section keeps the 150 MHz local oscillator in phase with the incoming carrier by controlling the phase of the 5 MHz NCO output which is mixed to produce the local oscillator. The symbol synchronization section keeps the symbol clock synchronized with the symbol periods of the incoming baseband signals. The automatic gain control (AGC) controls the amplitude of the baseband signals being sampled by the analog-to-digital converters. The lock detection provides a positive indication when the processor is synchronized to a legitimate data transmission. The transmit section consists of a scrambler to ensure a sufficient rate of symbol state changes and an encoder to resolve the ambiguity that derives from the rotational symmetry of the symbol vectors in the I-Q plane. (See detailed explanations below). The decoder and descrambler in the receive section provide the inverse functions of the encoder and scrambler.

The input to all of the algorithms of the baseband processor is the series of 6 bit digital samples of the analog baseband signals of the I and Q channels. The baseband signals are sampled eight times per symbol period. One of the eight samples occurs in the middle of the symbol period. This is the symbol sample. It is a digital measure of the symbol level which is decoded by the symbol detect circuitry. The four levels of a perfect baseband signal produce digital values of +24, +8, -8, -24 for the +3, +1, -1, and -3 levels respectively.

To understand the algorithms of the baseband processor, it is best to visualize the state of the baseband signals as one of 16 vectors in the I-Q plane (See Figure 5). For example, if the I level is +3 and the Q level is +1, then the corresponding vector points from the origin to the point in the lower right hand corner of the (+,+) quadrant. Its phase is $\tan^{-1}(1/3)$.

The carrier synchronization algorithm compares the phase angle of the observed symbol vector with the phase of the expected ideal vector for the current symbol. For example, if the I and Q symbol samples are +27 and -6 respectively, the level detect circuits will detect (I,Q) equals (+3, -1) and the carrier synch circuitry will compare $\tan^{-1}(-6/+24)$ to $\tan^{-1}(-1/+3)$. The difference is scaled and used to control the phase of the 150 MHz local oscillator. The resulting phase-locked loop has a loop noise bandwidth of 50 MHz and a damping factor of 0.6. It is a perfect second-order loop.

The symbol synchronization algorithm is pictured in Figure 6. Samples of the I channel baseband are summed from the center of one symbol period to the next. If a symmetrical transition (i.e., +1, to -1, -1 to +1, +3 to -3, or -3 to +3) occurred during that time the result should be zero. If the result is not zero, then the of the sum, along with the direction of the transition, indicates whether the symbol clock is lagging or leading the received symbol rate. If a number of successive measurements indicates the same direction of clock phase error, a threshold detector will adjust the symbol rate. The symbol clock is generated by the

most significant bit of a 4-bit counter that is clocked at 16 times the symbol rate. A lagging clock is adjusted by decreasing the count per symbol period to 15 for one period. A leading clock is adjusted by increasing the count per symbol period to 17 for one period.

The automatic gain control computes the difference between the absolute value for the symbol sample and the absolute value of the expected ideal sample value. This difference is accumulated for 16 symbol periods. The result is summed with the current gain control level to change the gain of the variable-gain amplifier.

The lock detection circuitry computes the same difference as the AGC, but accumulates the absolute value of this difference for 16 symbol periods. If the result is less than a lower threshold, a 3-state counter (i.e. counts 0, 1, and 2) is incremented. If the result is greater than an upper threshold, the counter is decremented. When the counter transitions from 1 to 2, the lock indicator is turned on. If the counter transitions from 1 to 0, the lock indicator is turned off.

The 4-bit symbols are encoded as shown in Figure 7 [12]. The upper two bits are encoded differentially by indicating the change in quadrant from the previous symbol. The lower two bits are coded by position within the quadrant. The differential encoding is necessary because the demodulator cannot distinguish among the four phases of the carrier. For example, if the previous transmitted vector was in the (+,+) quadrant and the current data is 0110, then the encoder will cause a (+1, -3) vector to be transmitted. The receiver may distinguish any of the following combinations:

Previous Quadrant	Current Vector	Quadrant Change
(+,+)	(+1,-3)	$+90^{o}$
(+,-)	(-3,-1)	$+90^{o}$
(-,-)	(-1,+3)	$+90^{o}$
(-,+)	(+3,+1)	$+90^{o}$

In all four cases, the correct data (0110) is decoded.

The scrambling algorithm [17] is essentially an exclusive OR combination of the 20th previous, 3rd previous, and current data bits. In addition, the polarity of the output is inverted whenever four consecutive 8-bit output sequences are identical.

CONCLUSION

The design of the 6402 High Speed Modem was accomplished using state-space simulation techniques for performance verification. Each of the elements in the receiver and modulator were modelled and tested completely prior to the hardware development. Laboratory tests have provided further verification using Scientific-Atlanta's 400 MHz headend and distribution system. The frequency-agile point-to-point modem represents a strong choice for high-speed communications over cable, with its bandwidth efficiency maximizing the spectral utilization of the coaxial cable system. The modulation scheme, QASK-16, selected for the 6402, is an excellent compromise between bandwidth efficiency and performance without leading to prohibitive manufacturing costs. Through novel design the 6402 achieves 2b/Hz spectrum efficiency using reliable, low-cost components.

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REFERENCES

[1] R.E. Pidgeon, Performance of a 440 MHz; 54 Channel, Cable Television Distribution System", 30th Annual NCTA Convention Technical Papers, 1981.

[2] C.M. Thomas, "Amplitude-Phase-Keying with M-ary Amphabets: A Technique for Bandwidth Reductions," Proc. Int. Telemetering Conf., October 1972, p. 289.

[3] J.G. Smith, "On the Feasibility of Efficient Multi-Amplitude Communication", National Telecommunications Conf. Rec., 1972, p. 20E-I.

[4] G.J. Foschini, R.D. Gitlin, and S.B. Weinstein, "On the Selection of a Two-Dimensional Constellation in the Presence of Jitter and Gaussian Noise", Bell Systems Tech. J., Vol. 54, pp 927-965, July-Aug. 1973.

[5] M.K. Simon and J.G. Smith, "Hexagonal Multiple-Phase-and-Amplitude-Shift-Keyed Signal Sets", IEEE Trans. Comm., Vol. COM-21, pp 1108-1115.

[6] F.J. Foschini, R.D. Gitlin, and S.B. Weinstein, "Optimization of Two-Di-

mensional Signal Constellation in the presence of Guassian Noise, "IEEE Trans. Comm., Vol. Com 22, pp 28-38, January 1974.

[7] J.G. Smith, "A Review of Multiple Amplitude-Phase Digital Signals", IFTJ., Vol 1, pp 6-14, Jan.-Feb. 1974.

[8] C.M. Thomas, M.Y. Weidner, and S.H. Durrani, "Digital Amplitude-Phase-Keying with M-ary Alphabet", IEEE Trans. Comm., Vol. COM-22, pp 168-180, Feb. 1974.

[9] M. Washio and T. Itaya, "Expermental Study on a New 1.6 Gbps 16-Level APSK Modem," National Tel. Conf. Proceedings, 1977 pp 05:6-1 - 05:6-6.

[10] A.P. Clark and M.J. Fairfield, "Detection Processes for a 9600 bit/s Modem", The Radio and Electronic Engineer, Vol. 51, No. 9, pp 455-465, Sept. 1981.

[11] W.J. Weber,III, P.H. Stanton, J.T. Surnida, "A Bandwidth Compressive Modulation System Using Multiple-Amplitude Minimum Shift Keying MAMSK)", IEEE Trans. on Comm., Vol. COM-26, pp 543-551, May 1978.

[12] W.J. Weber, III, "Differential Encoding for Multiple Amplitude and Phase Shift Keying Systems", IEEE Trans. on Comm., Vol. COM-26, pp 385-391, March 1978.

[13] M.K. Simon and J.G. Smith, "Carrier Synchronization and Detection of QASK Signals",IEEE Trans. on Comm., Vol. COM-23, pp 606-620, June 1975.

[14] M.K. Simon, "Data-Derived Symbol Synchronization of MASK and QASK Signals", IEEE Trans. on Comm., Vol. COM-23, pp 606-620, June 1975

[15] M.K. Simon, "Data Derived Symbol Synchronization of MASK and QASK Signals, "Jet Propulsion Laboratory, Pasadena, Cal., JPL Tech. Memo 33-720, Dec. 15, 1974.

[16] W.J. Weber, III, "Decision-directed Automatic Gain Control for MAPSK Systems", IEEE Trans. on Comm., Vol. COM-23, pp 510-517, May 1975,

[17] C.C.I.T.T. Recommendation V.35, App. 1.

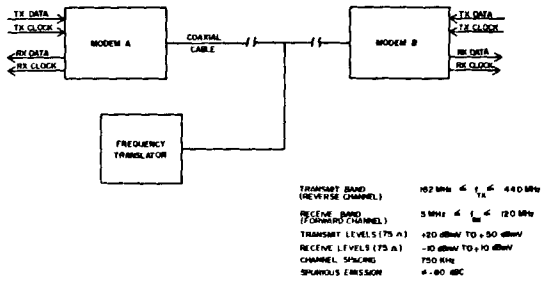

FIGURE 1 COMMUNICATION SYSTEM CONFIGURATION

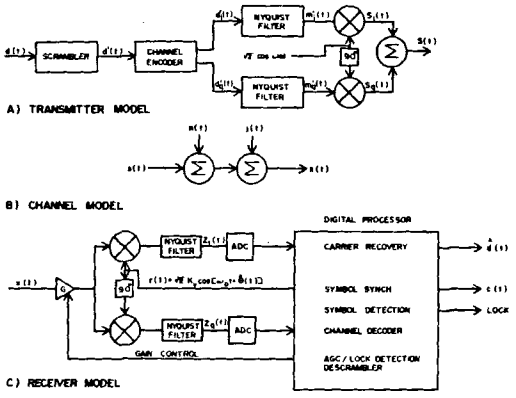

FIGURE 2 SYSTEM MODELS

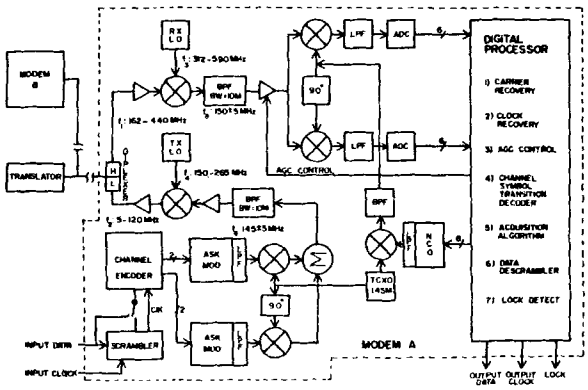

FIGURE 3 QASK MODEM FUNCTIONAL BLOCK DIAGRAM

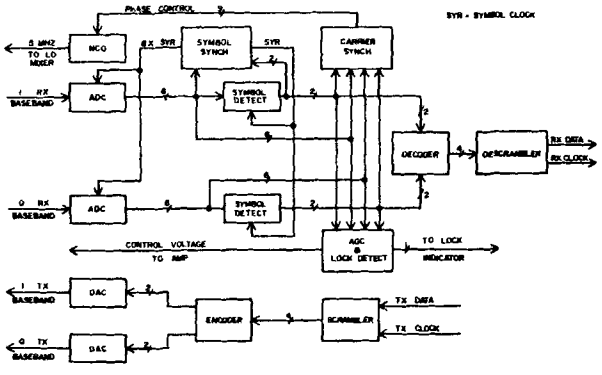

FIGURE 4 BASEBAND PROCESSOR

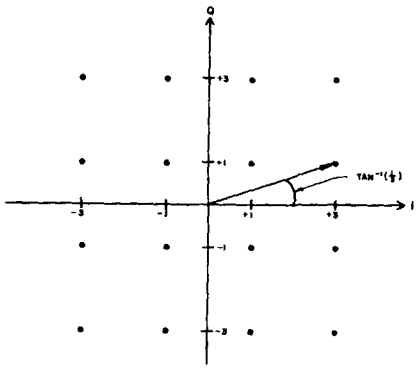

FIGURE 5 SYMBOL VECTORS

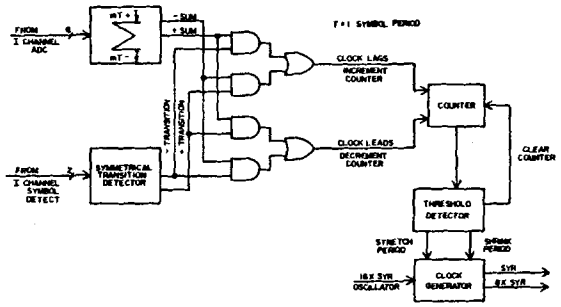

FIGURE 6 SYMBOL SYNCHRONIZATION

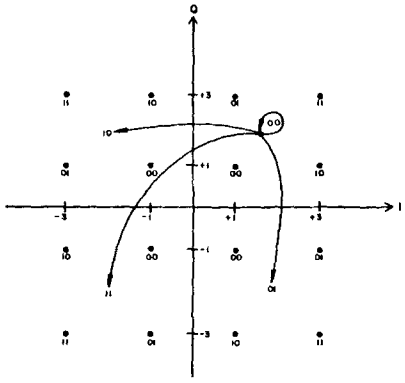

FIGURE 7 SYMBOL CODING