SYSTEM DESIGN CRITERIA OF ADDRESSABLE TERMINALS OPTIMIZED FOR THE CATV OPERATOR

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Pay TV has now emerged as a primary driving force for the rapid expansion of CATV subscriber growth. Effective control of subscriber access to premium programs can be realized through the availability of low cost subscriber terminals, capable of remote authorization of multi-tier subscription and eventually pay per view services. Providing reliable terminal equipment with increased capability at low cost, represents both a challenge and an opportunity for CATV manufacturers. The limitations of the traditional approach to data distribution are examined and compared to the emerging trends in newer system designs. The trade-offs and specific solutions to the problems of authorization speed and data format are presented. A headend distributed computer architecture is also discussed which results in lower initial cost and overhead while permitting the multiple system operator to exploit the advantages of simplified on-site upgradability and reduced spare part inventory. Technqiues which permit simplified, cost effective solutions to the problems associated with cable system growth, are also discussd.

INTRODUCTION

Sync suppression has long been recognized as an effective method of limiting subscriber access to premium programs. A key factor in the viability of this technique is the proliferation of new pay services and the ever increasing cost of service changes.

Advanced system design strategies are required in order for manufacturers to meet the demand for increased capability while avoiding product obsolescence and higher cost.

Remote authorization subscriber terminals requires the transmission of data to control the re-insertion of timing which was deleted from the video signal, identify the tier or pay level of premium programs, and address, authorize and connect (or disconnect) the terminal. Addressability is based on transmission of the required data in two ways: timing and level information is present on an additional modulation component contained within the normal 6 MHz TV signal, while authorization and connection data is sent on a separate narrow band FM carrier.

TIMING TRANSMISSION

While the limiting action of the TV receiver rejects the added timing signal, it is present at the channel converter output for use by a timing signal receiver. The receiver identifies the channel by detecting a set of pulses called a "tag". Note that the tag does not identify the TV channel number, rather the tier or pay level of the transmission on that channel. The tag pulses are binary coded to specify 1 of 128 possible levels.

DATA TRANSMISSION

Preliminary results of experiments with multi-level addressable descramblers, have generated concern with respect to update rate, error performance, bandwidth requirements, and cost of both terminals and headend equipment. Of secondary importance, is the lack of standardization and compatibility between systems designed for the same or similar purposes.

The traditional method of distributing authorization codes is to simply send the configuration of address, authorization data, and control bits as one data word as shown in Figure 1. In this example, 35 bits are

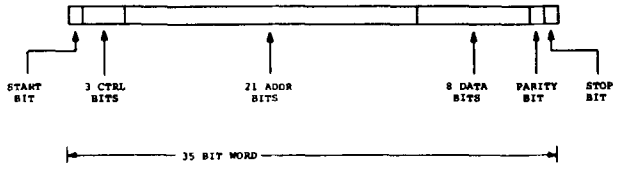

Figure 1

Traditional Word Format

necessary to completely define the transmission to each individual terminal. This method has the advantage that all of the information intended for a given terminal is contained within the space of one transmitted word. Some disadvantages are: the check (parity) and sync bits occupy only 8% of the word, resulting in reduced detection capability; system update rate is slow because most of the information is repeated from one word to the next, and both the terminal and headend re-

quire expensive dedicated hardware because of the non-standard nature of the word format.

The disadvantages may be overcome by a unique collection of techniques oriented toward the standard EIA word format shown in Figure 2. The address, control and

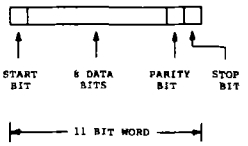

Figure 2 EIA Word Format

authorization data are partitioned into groups, and transmitted sequentially. The terminal receives each word in sequence, compares its logical address to the designated group, and stores the result for subsequent use. No action will occur until all groups have been validated. The control bits would be used to command all terminals to perform the same action; therefore, the command word need be sent only once during a sequence.

This concept offers the ultimate in flexibility, yet maintains compatibility with all industry accepted data communication protocols. The logic required to identify, interpret and respond correctly to so complex a transmission sequence would not be cost effective were it not for the availability of microcomputer and LSI circuits. Designing an addressable converter/descrambler using microcomputer technology represents both an opportunity and a challenge due to the complex nature of these devices.

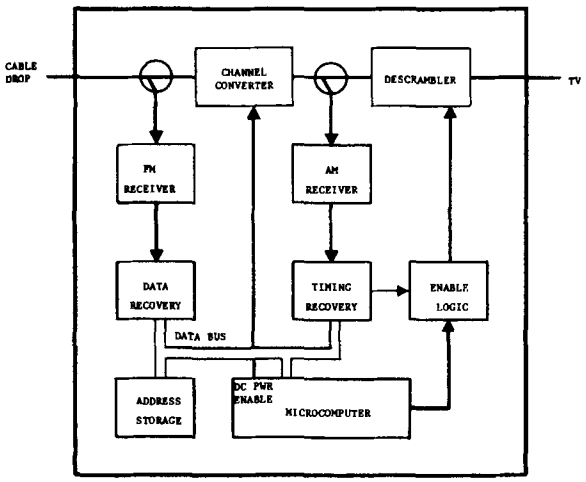

Figure 3
Addressable Converter/Descrambler Block Diagram

The diagram in Figure 3 illustrates a typical design. The FM receiver demodulates the data and converts it to a serial bit stream. The data recovery circuit synchronizes and decodes the bit stream, presenting 8 bit parallel data to the microcomputer for analysis. The AM receiver demodulates the timing signal which is decoded by the timing recovery circuit to generate the composite sync signal. The address, authorization, connect and level data is analyzed by the microcomputer which responds by controlling the converter and descrambler circuits.

The requirement to uniquely identify each terminal is of special importance when viewed in the light that hundreds of thousands of terminals may exist on a single cable system. This problem may be solved by using a programmable read only memory to store the terminal's logical address. Terminals may be shipped from stock and inventoried as identical units because addresses are assigned at the time of installation.

Figure 4 typifies the performance possible in this type of addressable converter/descrambler design.

• Address range	:	2 million subscriber terminals
Geography code	:	8 cable systems
Terminals	:	256K per system
• Update rate	:	128K subscribers
8 Levels	:	4 minutes
• Timing transmission	:	Embedded in TV signal
Program levels	:	128
• Data transmission	:	Narrowband FM
Frequency	:	107.3 MHz
Level	:	-15 dB below picture carriers
Guard band	:	±200 KHz
• Features		
Microcomputer architecture		
EIA compatible data format		
High performance/cost ratio		

Figure 4
Addressable Converter/Descrambler Performance Summary

HEADEND

Improved utilization of headend resources is also possible through exploitation of microcomputer devices in the form of distributed computer architecture. Within this concept, a microcomputer is used to store, format and transmit the address, control, and authorization data to the RF data modulator. Because of its small physical size and dedication of purpose, the microcomputer can be designed to fit within the main frame of a controller computer as shown in Figure 5. The microcomputer module is purposely limited to servicing a reasonably small number of terminals and levels to keep initial cost low. As system penetration increases or it becomes advantageous to increase the number of levels (or both), additional modules may be added. This technique more closely re-

lates headend cost to generated revenue and permits growth through upgradability instead of replacement, while lowering maintenance cost due to reduced spares inventory.

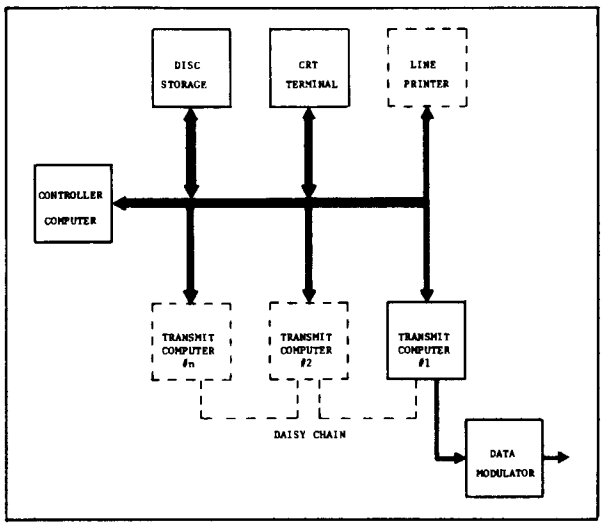

Figure 5
Controller Computer Architecture

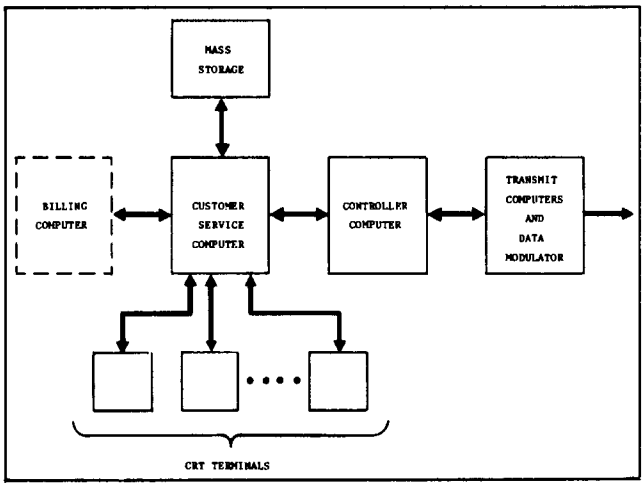

Figure 6
Distributed Computer Architecture

The controller computer, freed from the task of transmitting data, is more effective in other system activities such as authorization file maintenance, terminal logistics management and auditing, and the creation,deletion and execution of authorization schedules. When the level of system activity warrants additional processing power, the distributed computer concept easily extends to customer service functions as shown in Figure 6. The customer service computer carries out the activities associated with cable system management and administration while directing control functions to the control computer as before. Transactions are acquired on line and recorded for subsequent use by a billing computer. The physical location of the billing computer may vary according to system requirements, however, the extension of the multiple computer complex to the inclusion of billing represents the final realization of distributed computer architecture, applied to the operation and management of the cable system.

SUMMARY

It has been demonstrated that the strategy necessary to produce higher cost effectivity in newer designs hinges on being able to exploit the advantages of low cost integrated circuit devices, in particular, those originally intended to serve the microcomputer industry, and that these devices hold the potential for performance improvement and lower cost in both headend and terminal equipment. Finally, the system design concepts presented should lead to products with the capacity to serve the needs of today and remain viable through upgradability in the future.