MICROPROCESSOR CONTROL FOR CATV TEST INSTRUMENTS

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ABSTRACT

The unique measurement requirements of our industry have, in the past, been served by general purpose test instruments requiring a high degree of operator interface and understanding. As technology advances, the microprocessor will smooth this interface and improve operating efficiency. Microprocessors allow us to configure an instrument to handle our unique requirements. Application of the microprocessor in the design of a new simultaneous-sweep system will emphasize the areas of improvement made possible by the use of this versatile component. The use of microprocessor control allows us to get the most useful information for the time spent testing. Areas where the microprocessor has had considerable influence are: minimization of the number and types of controls, digital storage of sweep response, communication between instruments, and post processing of response data. These areas will be discussed in some detail, along with the idea of upward expandability.

INTRODUCTION

Test instruments must provide the operator with some useful source of stimulus, the means to analyze an output from a device under test, or a combination of the two. In the past, high-frequency test instruments were general in concept, covering functions with broad market appeal. The unique requirements for CATV test instruments had to be realized with equipment which was not specifically designed for that purpose. Some of the compromises included frequency ranges, physical construction, and excessive operator control interface. Early instruments had complex mechanical linkage for tuning and gain control. More accurate instruments used hand-calibrated scales to compensate for component variation.

As varactors, pin diodes, and integrated circuits found their way into instruments, performance improved, more functions could be implemented in a given volume, and the front-panel controls become a complex of push-buttons, back-lighted rotary switches, digital readouts, and slide-rule dials. This continued until it was difficult to find the power switch in the maze of controls. These complex control panels allowed flexibility, but required an operator with a high degree of proficiency.

As we see it, the concept of microprocessor control reduces the complexity of the control panel and simplifies operator interface. The operator interface can now be "human engineered" with keyboard entries and alphanumeric readout of results, error messages, and system status. Perhaps the most important innovation of the microprocessor to instrument design is the fact that, because the instrument is a general set of hardware with a software instruction set, the software can be configured for specific instrument requirements with little or no change in hardware.

THE MICROPROCESSOR IN A NEW SIMULTANEOUS–SWEEP SYSTEM

There exists a trade-off in sweep response accuracy and potential interference to customers. We have purposed and conducted a study to show the subjective interference as a function of time in a channel with level and repetition rate as parameters. With data showing various optimum combinations of sweep level and in-channel time, the problem of broad-band vs. narrow-band recovery can be addressed.

Narrow-band recovery requires longer in-channel time and, therefore, low sweep level to satisfy the interference criteria. The resolution is minimal due to tracking bandwidth, especially in the areas of the channel carriers. Noise level is also a problem in longer cascades.

Broad-band recovery can utilize fast sweep time, but requires a higher level. The broad-band recovery method eliminates the tracking errors, reducing the problems to minimization of the sweep level and maximization of the resolution of the recovered response. Microprocessor control of the sweep transmitter and recovery systems is the key to solving these problems.

The microprocessor in the sweep transmitter allows the parameters to be entered via a keyboard and displayed on an LED readout. Inputs which are not in a programmed range are rejected. Valid inputs are used to set up digital-to-analog converters to control the sweep parameters.

The microprocessor uses a "look-up" table in memory to set the level in .1 dB steps. It also blanks the output and reads a counter at the beginning and end of the sweep period. Corrections are made via separate digital-to-analog converters, with the end frequencies nearly two orders of magnitude more accurate than obtainable with standard sweep generators.

Communication from the sweep transmitter to the recovery system receiver is by way of a carrier, phase-modulated with a serial ASCII code. Decoding at the recovery system tells the processor the start and stop frequencies, the sweep duration,

and the repetition rate. The recovery system accepts data if it passes parity and check-sum tests.

Following the data transmission, the sweep transmitter uses the data link to send a pair of pulses. The recovery system reads these pulses as "pass one" and "pass two". The timing of these pulses is precisely controlled by the transmitter microprocessor, and allows cancellation of common sync by the recovery system. At the recovery system, the microprocessor controls the selection of preamplifier gain, which will optimize the signal to noise ratio for the recovered response.

When operating at near-carrier levels, the detected sweep response tends to show variations which limit the resolution of the instrument. The microprocessor provides several means to improve this situation. As the signals from the combined channels are summed into the detector, they create a DC value and a complex AC waveform. The low-frequency components of this waveform, as well as temperature-related DC and bias drift, are eliminated by an automatic-zero control circuit. This circuit holds the output of the detector at a constant level until the microprocessor sends a command which causes the circuit to maintain its last correcting value. Measurements are then made from that constant reference level.

Elimination of DC and low-frequency errors leaves the problem of sync pulses from many channels. Taking advantage of the data link, the pass one and pass two pulses previously mentioned are used to subtract the sync pulses from the response, which allows the resolution bandwidth to be maintained at a much higher value.

The recovery system reacts to the pass one signal, and converts a series of samples to digital data which are stored in sequence by the main random access memory. The timing from pass one to pass two is controlled so as to be within 1 usec of TV frame time. At pass two, the recovery system again converts a series of samples, but this time the sweep is also present. The difference between these two series of samples replaces the sequence in memory, which is recalled at a 60 Hz rate to refresh the CRT display. Since response data is stored in sequence, display timing and some logic controlled by the microprocessor can be used to convert the digital data back to an analog response at the CRT without using a special digital-to-analog converter.

After the recovery system has stored the sweep frequency response, the microprocessor inhibits the switch mode power regulators, powering down the RF section along with the analog-to-digital converter. The memory and CRT remain active as the timing circuits synchronize and refresh the display.

The recovery system processor uses the ASCII data to time out the sampled response. It also calculates the frequency and/or level of keyboard-controlled cursors as they are positioned on the display, the level being calculated as a function of a table in memory and the attenuator settings. When the Δ key is activated, the microprocessor calculates the difference between the two cursors. Results of these calculations are written on the CRT display in a format which is also controlled by the processor.

The microprocessor monitors the system and outputs error messages to the CRT such as: low battery, missing input, or attenuator changes.

Expansion of such a microprocessor-controlled instrument can be implemented by option cards or by interfacing additional packages via RS232 connectors.

Utilizing the microprocessor control and the data link, a system of this type can be set up to sweep the return system from a remote location back to the headend. At the headend or hub, the response can be coded on the data link and transmitted as data to the location under test, where it will be loaded into memory and displayed on the CRT.

Data in storage can be transferred from memory to magnetic cards or vice-versa with little change in the basic hardware. Memory can be added to perform digital averaging or normalization of response data.

The selection of a microprocessor for the sweep transmitter is based largely upon its support circuitry and software, while the main considerations for the recovery system microprocessor selection are low power consumption and its use of direct memory access.

DIGITAL DISPLAY STORAGE

Storage displays have typically been used to store information of the following types: the non-repetitive signal that would appear on a CRT momentarily, and then disappear; the signal that has a low repetition rate (usually below 40 Hz); and the low-duty-cycle signal that is too dim to observe. Until the early 1970's, the instrument manufacturer's solution to this problem was a storage-tube display. The storage-tube displays, while solving to some degree the problems previously described, left some problems to live with or still overcome. The displays would "flood" if the intensity were set too high or miss data if the intensity were set too low, and the cost would be higher than the standard CRT.

In the early 1970's, some of the instrument manufacturers began to develop digital storage displays. These displays are actually standard oscilliscope displays that are refreshed by semiconductor memories. The refresh rate is designed to be great enough to provide a flicker-free display.

The digital storage display provides some other advantages when combined with a microprocessor system. The stored data in the display memory can be accessed by the microprocessor and converted to a value easily read by the operator, and alpha-numeric characters may be combined on the screen with the displayed data. This provides the operator with easy access to the processed data and a convient readout of the instrument setting. Since the data is stored in a RAM (random-access memory), there is no fadeout of the displayed data as long as the instrument power is on. Another advantageous feature if temporary storage is available is the transfer of the display data to the temporary storage area. This allows the operator to read the data at some later time to compare with more recently acquired data. This concept can be taken another step, the display data being transferred to non-volatile magnetic storage (card or tape) to be evaluated weeks or months later. This data could also be used for statistical processing on a computer.

The typical digital storage display system centers around a random-access read/write memory. The access to the memory and the timing of both the input and output is under the

control of a control timing logic circuit. The input control and timing, as well as the type of analog to digital conversion performed, is a function of the type of signals to be converted. Some examples are: If the input data is slowly changing X-Y data, then both channels would probably be converted using tracking A-D converters, and a periodic sample window would be provided by the control timing logic circuit to the display memory; If the Y data is changing rapidly and the X input is a ramp, then a good approach is to use a tracking A-D converter on the X input and do a fast successive approximation conversion on the Y data whenever the X data changes; A third class of input signals to consider is a short burst of rapidly varying Y input data of a known duration, with the X input a timing pulse indicating the start of the Y data. In this case, the X input timing pulse may be used to reset a counter, and to cause the control timing logic to take access to the display memory away from the display and to give it to the input converter. At this time, the Y conversion takes place, the X counter is incremented, and the data is stored in memory. This cycle is repeated until the counter reaches it's final state, at which time the display memory access is passed back to the display.

The interface between the display memory and the display is dependent on the type of display used. Two that will be considered will be X-Y and raster scan. For the X-Y display, both the X and Y outputs come from D-A converters. The Y converter input is the display memory data, and the X converter input is the address of the data in the display memory. The control and timing logic increments to the next address. This process continues to the end of the display memory, when the address is reset to the start and the process is repeated.

In the raster scan, the memory data and address are converted to time intervals. The memory data is converted to a time interval from the bottom of the screen to the data dot. This conversion is made by loading the memory data into a counter and counting it down with the video clock during the upward trace of the beam. The data memory address is generated by a counter. The counter is advanced every vertical retrace, and is reset at each horizontal retrace.

DIGITAL SUBTRACTION

The storage of the data in digital form has provided us with an opportunity to improve the signal-to-background performance of our CATV Sweep Recovery System. The signals on the cable are nearly periodic at the TV frame rate. This may be taken advantage of by sampling the cable signal one frame prior to the sweep, then using this stored sample to subtract the background one frame later when the sweep is received. This is accomplished by transmitting two start-sweep pulses to the receiver. During the first pulse, no sweep is transmitted, resulting in the background being stored in the display memory. When the second pulse occurs, the sweep is transmitted. As the analog-to-digital conversions take place, the background data is read from display memory. This background data is converted to analog and subtracted from the input signal. The resulting difference signal is then converted to digital and stored in the display memory.

MICROPROCESSOR – CONTROLLED TIMING

The microprocessor is also used to control the major timing events of a system. In our recovery system, these major timing events are: the access of the operator to modify the system parameters (attenuation, cursor position, display mode, etc.); powering up the RF and A-D conversion circuitry and accepting the transmitter status; the receipt of the sweep data and processing of new cursor values for received data.

A time interval is made available to the operator by the processor to change the receiver status via the keypad. During this interval, the processor scans the keypad and responds to its commands. The length of this interval is derived from the sweep repetition rate data from the transmitter, and is converted by the microprocessor to the number of horizontal retraces to be counted.

When the processor has counted down the proper number of horizontal retraces, it quits scanning the keypad and applies power to the RF and A-D converter circuitry. The processor then samples a device which decodes the serial data sent from the transmitter on the pilot signal. The received data (sentinal character, start frequency, frequency span, sweep duration, sweep reptition rate, and check-sum) is stored in the processor memory. For the data to be considered valid, both the byte parity and check-sum must match. If the data received is not valid, it is ignored, and the previously received transmitter settings are used.

After the transmitter status data is received, the display memory control timing circuits are activated to receive the "pass one" and "pass two" sync pulses. The processor scans the control timing circuit waiting for an indication that the frequency sweep has been received. Upon receipt of the sweep, the processor turns off the power to the RF and A-D circuitry, and calculates new cursor values based on the received information.

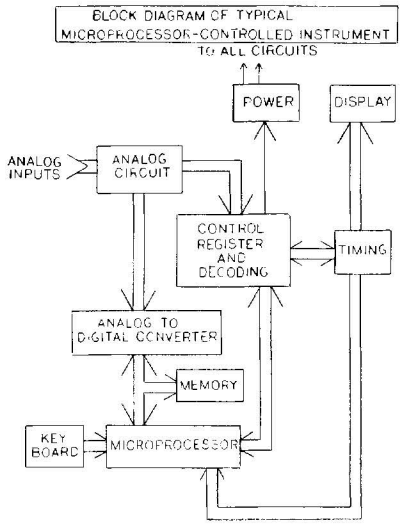
The microprocessor is limited in respect to the speed at which it can provide timing signals to the system. The vertical timing interval for the recovery system is an approximately 63 microsecond period. This interval is divided into 457 video clock cycles of about 140 nanoseconds each. The timing of the vertical information (characters, grid, data, cursors, and retrace) is controlled by discrete logic that operates at nanosecond switching speeds. Even some of the horizontal timing (request for new characters, grid, cursors, and retrace) is provided by discrete logic. The processor does aid in the horizontal timing by providing direct memory access for the display data, supplying the new characters when requested, and by resetting the direct-memory-access counter and character counter during horizontal retrace. These two counters reside in the memory of the microprocessor.

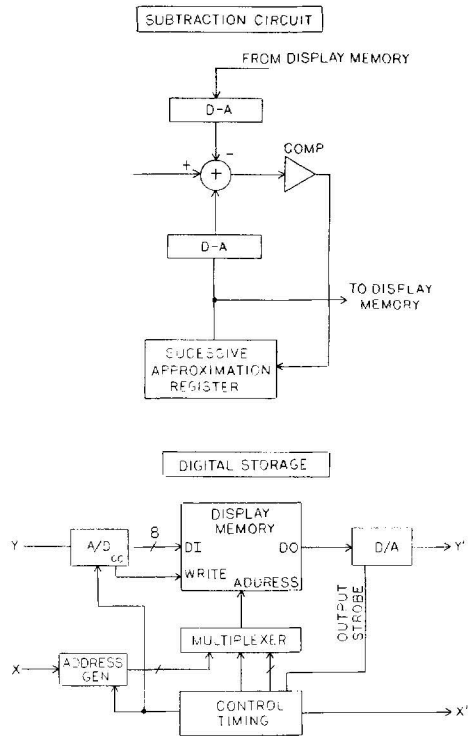
OPERATOR INTERFACE

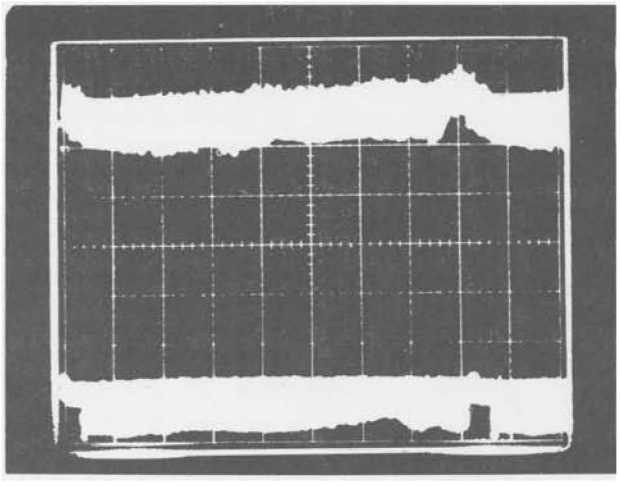
The operator interface for a microprocessor-controlled instrument may be made relatively simple, particularly when the instrument has alpha-numeric readout on a display CRT.

The system setting resides in the microprocessor memory. This allows the used of a simple matrix keypad instead of many rotary switches on the front panel. This keypad, along with the switches on the attenuator shaft, are connected to the microprocessor in such a way that the processor sees them as an extension of its internal memory.

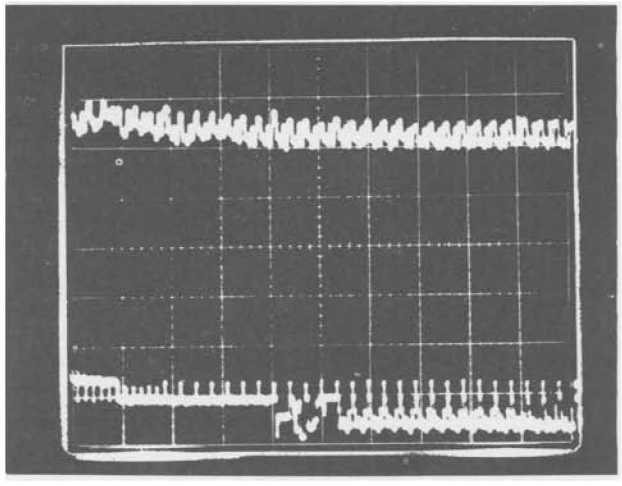
The microprocessor (and its memory components) has made available to the designer the tools to design complex logic systems at low cost and small size. These same designs 10 years ago would have been at least an order of magnitude more costly, with approximately the same increase in size.



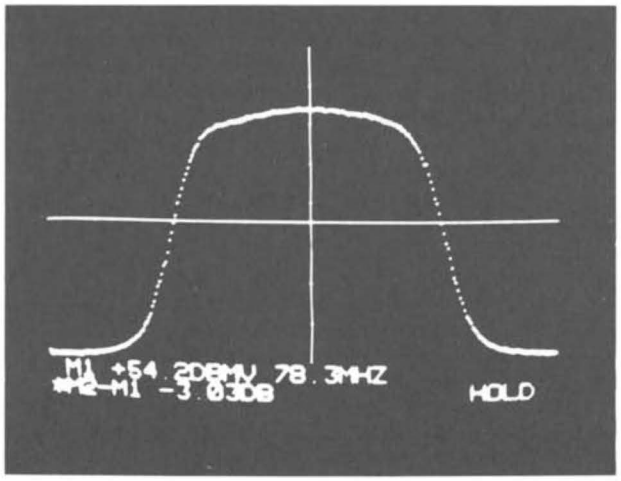




DETECTED OUTPUT FROM 12-CHANNEL SYSTEM.
CENTER LINE = GND. HORZ = 2 msec/div.
BOTTOM TRACE IS VIDEO FROM SINGLE CHANNEL USED TO TRIGGER SCOPE.



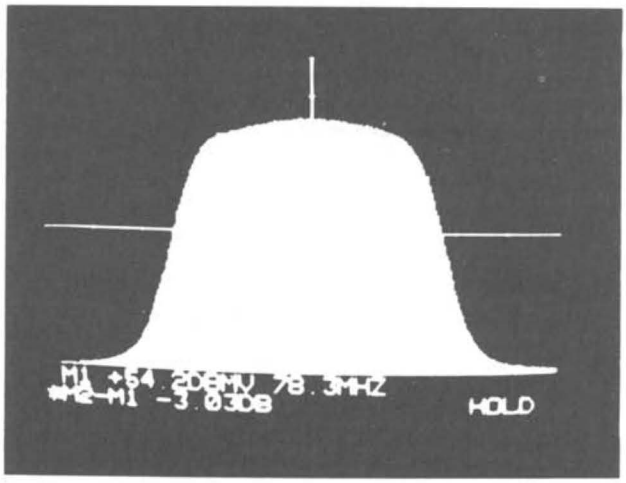
DETECTED OUTPUT FROM 12-CHANNEL SYSTEM.
CENTER LINE = GND. HORZ = .2 msec/div.
BOTTOM TRACE IS VIDEO FROM SINGLE CHANNEL USED TO TRIGGER SCOPE.



DOT MODE DISPLAY OF STORED DATA SHOWING LEVEL AND FREQUENCY CURSORS WITH ASSOCIATED ALPHANUMERIC DATA.

"M2 - M1" (Δ) INDICATES THE DIFFERENCE BETWEEN LEVEL AT CURSOR M2 (HORIZONTAL) AND LEVEL AT CURSOR M1 (VERTICAL).

"HOLD" INDICATES SYSTEM STATUS.



LINE MODE DISPLAY OF STORED DATA SHOWING LEVEL AND FREQUENCY CURSORS WITH ASSOCIATED ALPHANUMERIC DATA.

"M2 - M1" (Δ) INDICATES THE DIFFERENCE BETWEEN LEVEL AT CURSOR M2 (HORIZONTAL) AND LEVEL AT CURSOR M1 (VERTICAL).

"HOLD" INDICATES SYSTEM STATUS.