SIGNAL PROCESSING REQUIREMENTS FOR MODERN CABLE SYSTEMS

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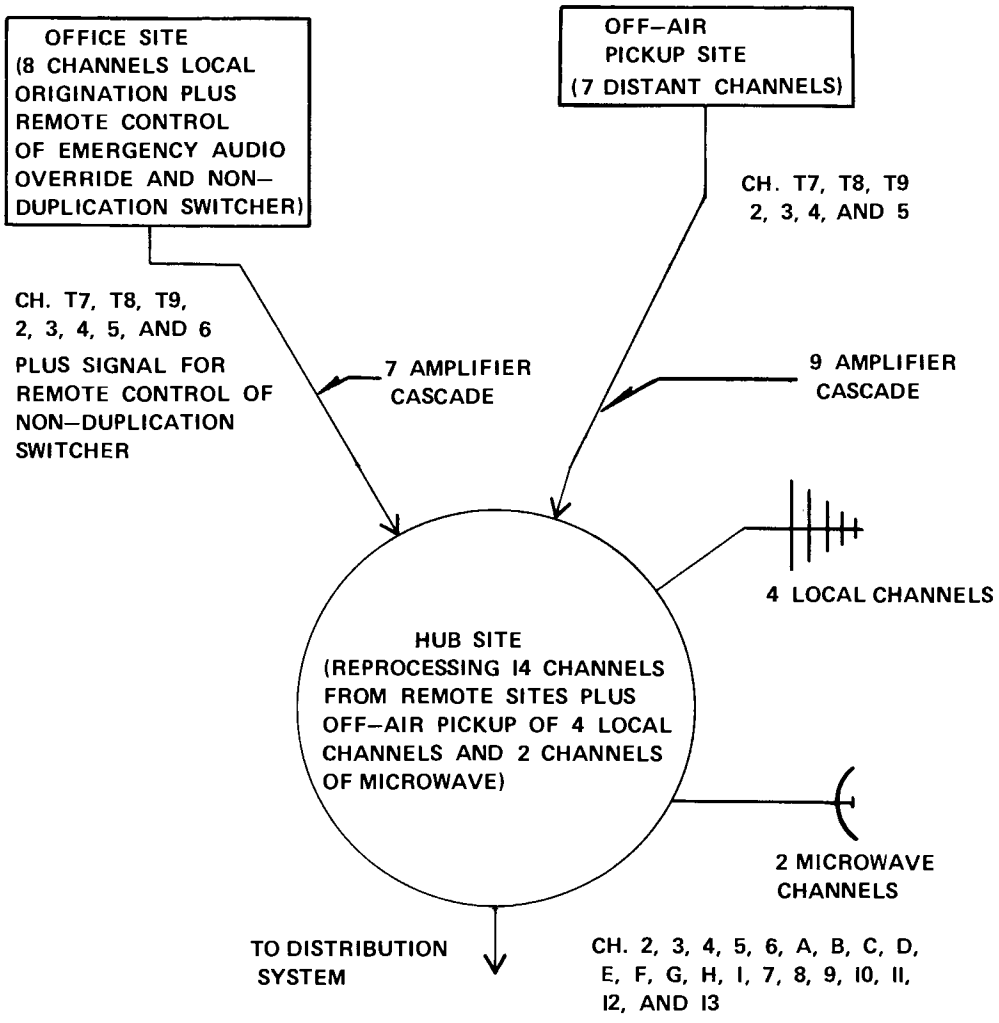
The movement of cable TV over the past few years from the rural areas into the large metropolitan areas has brought with it new demands on the techniques of processing signals. To a large degree these changes in processing requirements have been dictated by the fact that in metropolitan areas, the best geographical location for receiving signals off-air is separated by some distance from the most convenient office and local origination site, and in most instances both of these are located some distance from the optimum point to distribute the signals. Headend electronics capable of operating in this environment without producing excessive degradation have increased the technical performance specifications of headend equipment, especially heterodyne signal processors. To investigate these increased performance demands, consider a "typical" headend system for a metropolitan area such as the one shown in Figure 1.

FIGURE 1 TYPICAL HEADEND SYSTEM FOR A METROPOLITAN AREA



Here we have the situation discussed above, where the office and local origination site, off-air pickup site, and hub site are physically located several miles apart. The processing problem arises at the hub site, particularly with the channels from the other sites that must be reprocessed. For the sake of discussion, let us consider the channel 3 signal being fed into the hub site from the off-air pickup site. This channel was originally received off-air as a standard VHF or UHF signal and converted to channel 3 in a signal processor. After combining with the sub-low and low band channels, it is fed through a 9 amplifier dedicated distribution system to the hub site. Here the combined signal is split as many times as there are channels coming in and fed into the input of a second processor. In this discussion we will assume that the channel 3 coming from the off-air pickup site will be carried on channel 3 on the distribution system. This being the case the signals present at the input to the channel 3–3 processor at the hub site will appear as in Figure 2.

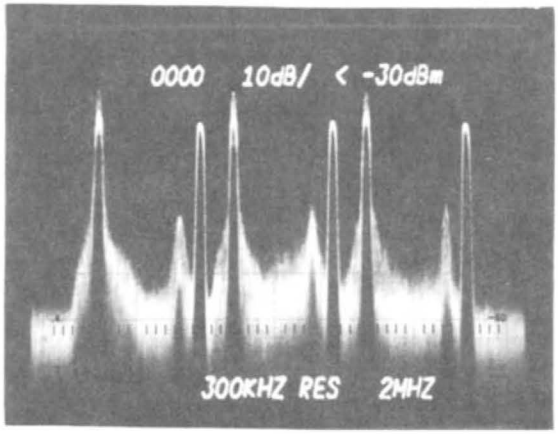


Figure 2. Ch 2, Ch 3, Ch 4 out of seven channels coming from off-air receiving site.

Here we show only three out of the seven signals that are actually present. For purposes of demonstration the sound carrier levels have been set 6 dB below the video carrier levels when in actual practice they are set approximately 15 dB below. The question here is: how much adjacent channel rejection must this processor have in order not to interfere with other channels being distributed on the cable? The worst case problem would exist if the channel 4 signal being distributed on the system is different from the channel 4 signal present at the input to the channel 3–3 processor. Under these circumstances, any of the channel 4 signal from the
through the channel 3–3 processor would fall back on channel 4, with an unavoidable frequency difference between it and the channel 4 distributed on the system. In this case 60 dB would be the minimum adjacent channel rejection allowable. In Figure 3 we show the amplitude response of a Scientific-Atlanta Model 6150 channel 3–3 processor. Here we see "notches" at the upper adjacent picture carrier frequency and lower adjacent sound carrier frequency in excess of 70 dB. We also see undesired but unavoidable "response upshoots" on the high frequency side about 20 dB down and on the low frequency side about 30 dB down. Would a processor with this

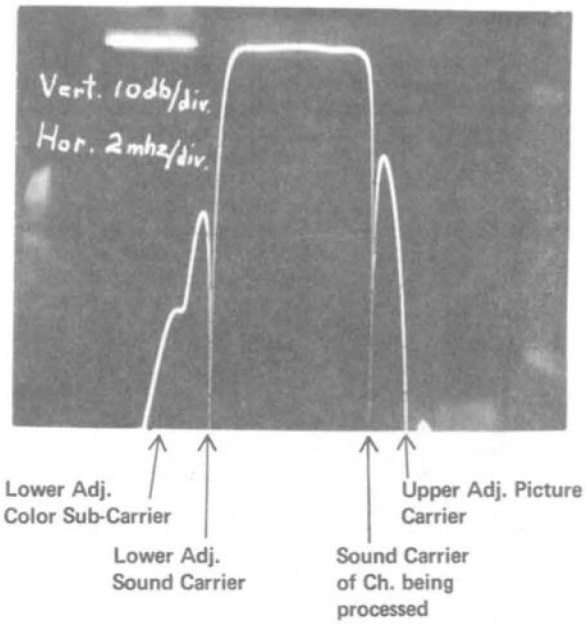


Figure 3. Amplitude Response of 6150 Signal Processor.

amplitude response be specified as having 60 dB adjacent channel rejection? Shown in Figure 4 is the output spectrum of this processor with the input spectrum shown in Figure 2. Here

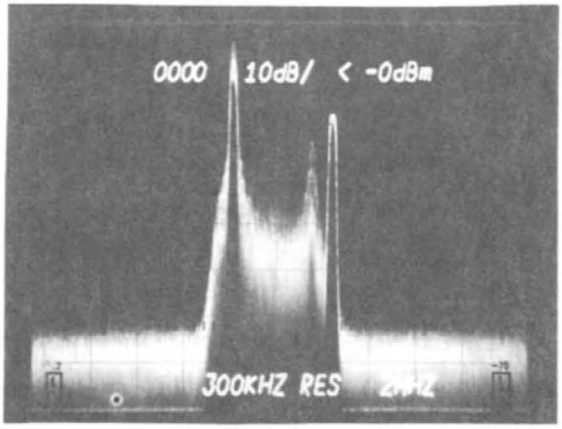


Figure 4. Output spectrum of signal processor with amplitude response shown in Figure 3 and input spectrum shown in Figure 2.

we see that there is no energy falling in the upper and lower adjacent channels greater than 60 dB below the desired video carrier level. Therefore, if we define adjacent channel rejection as the rejection to equal level adjacent channels that have "normal" energy distributions (pc = 0 dB, sc = -6 dB, cc = -17 dB), this amplitude response would have 60 dB adjacent channel rejection. The point here is that deep notches alone do not con-

stitute adjacent channel rejection. Nor does "response upshoots" necessarily hurt you. It is a combination of the processor amplitude response and the energy distribution of a "typical" television signal that together make up adjacent channel rejection. Signal processors with 60 dB adjacent channel rejection have only recently become available in the CATV industry. Before this, processors located at hub sites required external traps/filters to achieve this degree of selectivity.

It should be pointed out that any additional increase in selectivity does not come without penalty. The price we pay is an increase in the differential time delay across the passband of the processor. Shown in Figure 5 is the amplitude and envelope delay response of the IF section of a Scientific-Atlanta 6150 processor, without delay equalization. The IF portion of the processor constitutes the majority of the selectivity and therefore produces practically all the delay. In the CATV industry envelope delay is defined as the differential time delay between the picture carrier frequency and the color sub-carrier frequency. From Figure 5 we can see this is approximately equal to 130 nanosec. for the processor with no equalization. It is also interesting to note that although the "envelope delay" is only 130 nanosec., the total differential time delay from band edge to the center frequency is approximately 500 nanosec. It should be pointed out that for "minimum phase shift" networks, into which category virtually all headend equipment falls, the amplitude response uniquely defines the delay response.[1] Therefore, regardless of how the response shown in Figure 3 is obtained, the delay would be the same.

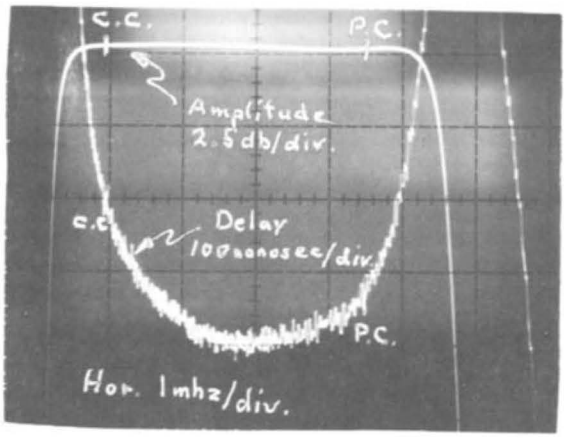


Figure 5. Amplitude and envelope delay response of IF section of 6150 processor (without delay equalization).

To determine the detrimental effects of processing signals through a device that has the delay characteristics shown in Figure 5, the test set up shown in Figure 6 was used. Here we

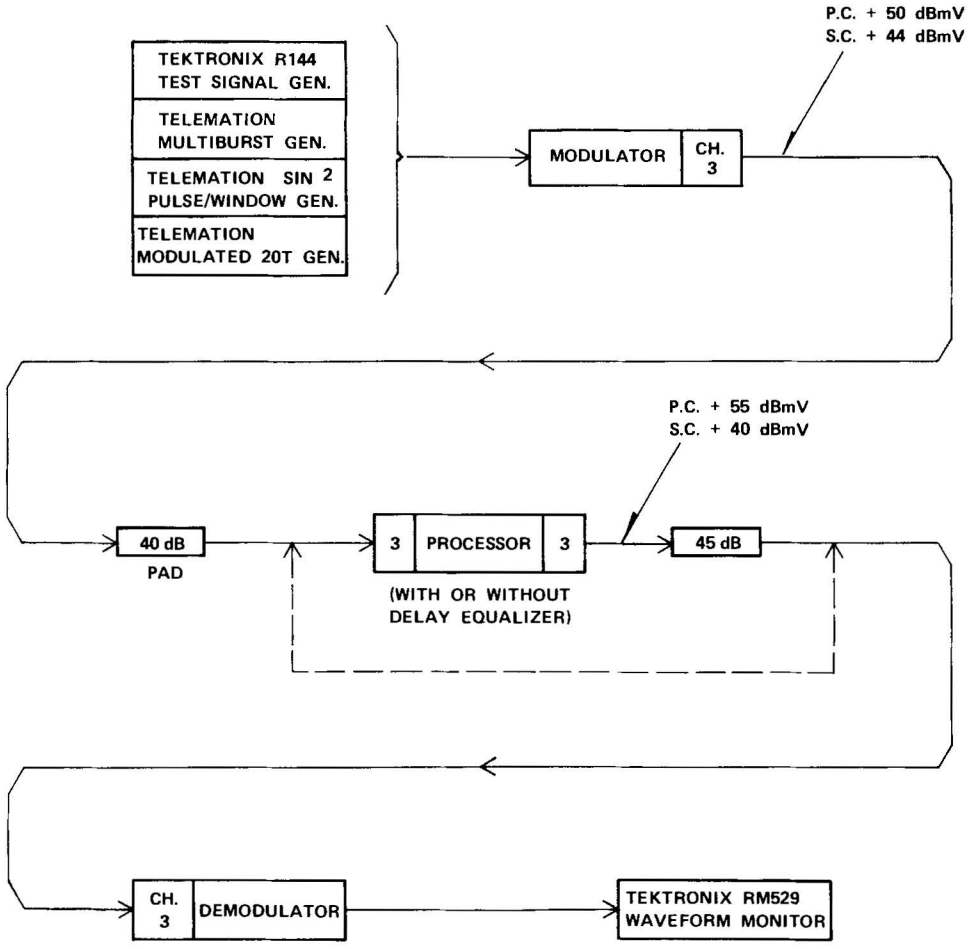
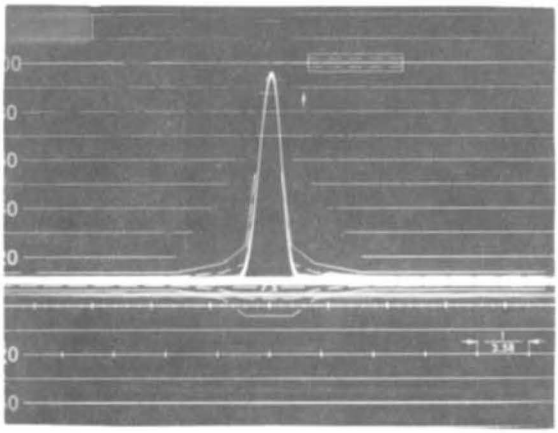
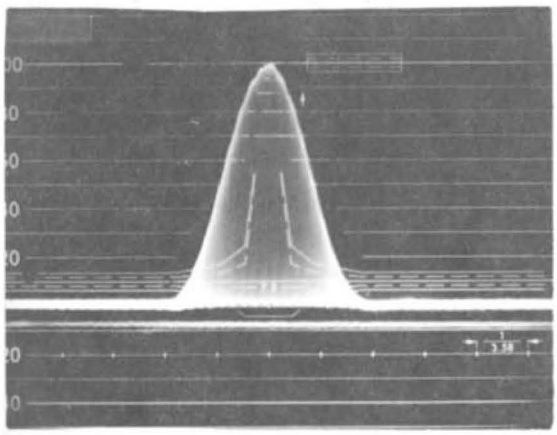


FIGURE 6 EQUIPMENT SETUP FOR WAVEFORM TESTING OF SIGNAL PROCESSOR

have a channel 3 modulator and channel 3 demodulator with the capability of either connecting them back to back or inserting the channel 3–channel 3 processor between them. Two video test signals were used in this evaluation, one being the "Modulated 20T pulse" and the other the "2T Sin² pulse." The first test signal was designed primarily to indicate the relative delay between the video carrier and the color subcarrier frequency. The "Sin² pulse" is more sensitive to the amplitude and delay in the vicinity of the response that the luminance signal energy occupies. Figure 7 shows the response of the modulator–demodulator back to back for the two test



K factor
≈2%
2T Sin² Pulse



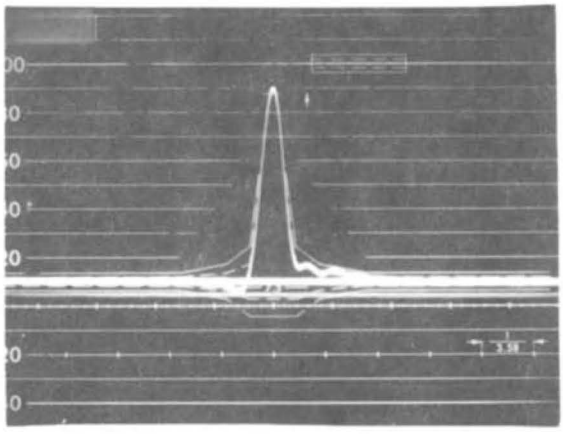
Envelope Delay
≈0
Modulated 20T Pulse

Figure 7. Video test signal response of modulator–demodulator.

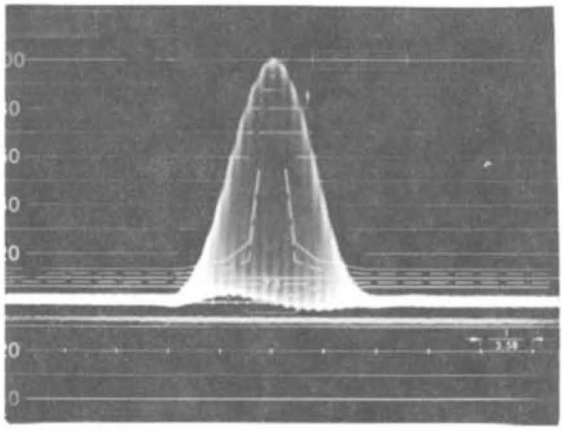
signals described above. As can be seen, the modulator–demodulator combination is very transparent, indicating very little distortion. The "Modulated 20T pulse" indicates virtually no envelope delay and the "Sin² 2T pulse" has a K factor of 2%.

Shown in Figure 8 is the result of passing these test signals through the same mod–demod, but with a 6150 processor with no delay equalization inserted between them. The distortion

off-air pickup site feeding



K factor
≈3.5%
2T Sin² Pulse



Envelope Delay
≈110 nanosec
Modulated 20T Pulse

Figure 8. Video test signal response of modulator – processor (without delay equalization) – demodulator.

passing through only one processor with no delay equalization. In headend-hub systems many signals pass through two processors. In this case the envelope delay would become approximately 220 nanosec. and the K factor would increase by

lization. From the amplitude response we see that although the all-pass delay equalizer is theoretically a lossless device, it does introduce a small amplitude variation (±.3 dB typical). Actually, the delay equalizer alone produces a 5 or 6 dB dip in the response which must be amplitude equalized to achieve the desired flatness. The results of passing the multiburst test signal first through the mod-demod back to back and then through the mod-processor (with equalizer)--demod can be seen in Figure 10. As evident from this photograph, the amplitude variation

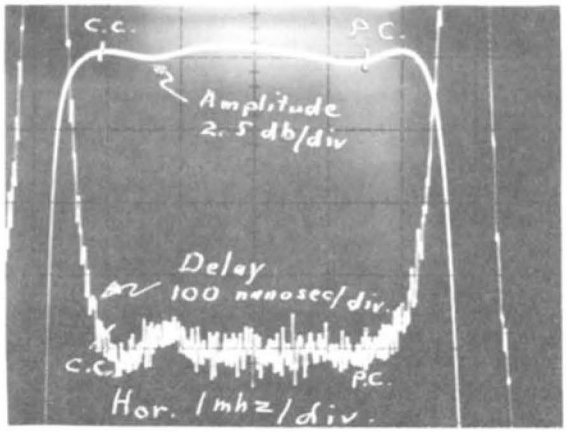
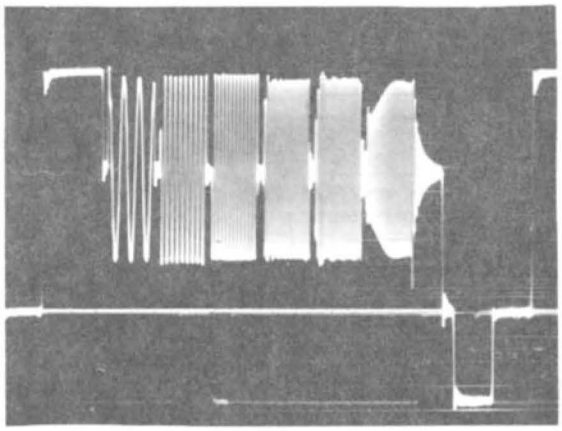
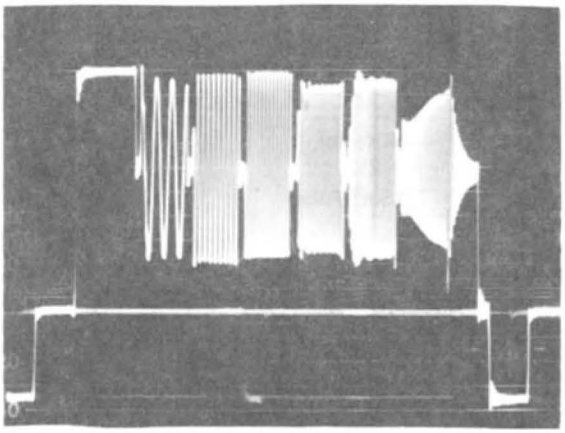


Figure 9. Amplitude and envelope delay response of IF portion of 6150 processor (with delay equalization).



Modulator–Demodulator



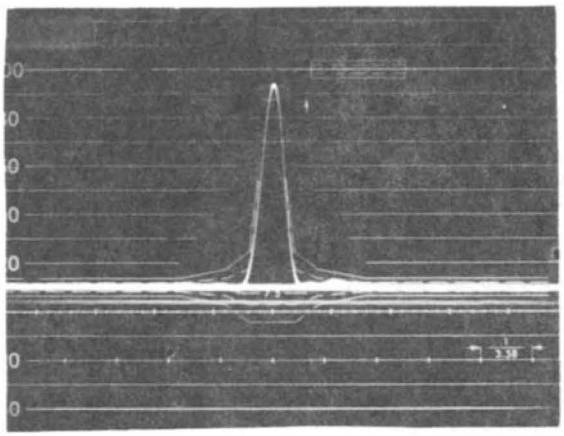
Modulator – Processor (with delay equalization) – Demodulator

Figure 10. Multiburst response of modulator – demodulator and modulator–processor (with delay equalization) – demodulator.

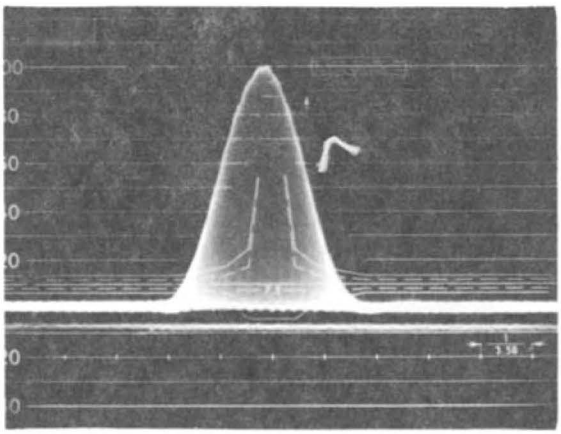
is certainly tolerable. Obviously, when comparing Figure 9 and Figure 5, the most dramatic difference caused by the delay equalizer is in the flatness of the envelope delay response. From this response it can be seen that the relative delay between the video carrier frequency plus .5 MHz and the color sub-carrier frequency is flat ±20 nanosec. Also evident is that from the two frequencies mentioned above to the band edges the delay is approximately 200 nanosec. The reason for this compromise in equalized delay is two-fold: first, the increase in complexity in an equalizer to achieve a flat delay from band edge to band edge would be tremendous. Such an equalizer would prove to be prohibitive not only from an alignment standpoint but also from a physical size standpoint, not to mention the problem of amplitude equalizing the device. Second, and even more important, the additional degree of improvement that would be obtained by complete equalization is negligible, compared to

the improvement already achieved. This can be seen from Figure 11. Here we see the results of sending the Modulated 20T and Sin^2 2T pulse test signals through the mod-processor (with equalizer)–demod. Note that the degree of distortion to the base line of the 20T pulse is virtually nonexistent, indicating, as is already evident from the swept delay curve, that the differential envelope delay at the video carrier frequency and color sub-carrier frequency is zero. Even more important however, is the complete lack of undershoot and trailing smear that was evident when there was no processor equalization. This is due to the flat delay in the vicinity of the video carrier. Comparing Figure 10 to Figure 7, it is apparent the processor with equalization is transparent to the test signals discussed above.

Now that we have an equalized processor, with 60 dB of adjacent channel rejection, does not insure that the use of external traps and filters can be eliminated. Discussed earlier in this article is the fact that at the hub site many processors will have as inputs the desired signal plus many more, including equal level adjacents. To insure that no external traps/or filters are required at the input of each processor, it must have the capability of "handling" these signals without generating in-band intermodulation. This distortion could occur in any active stages prior to removal of the adjacent channels and once generated, no amount of adjacent channel rejection can remove it. To demonstrate this problem, I combined the output of a channel 2, channel 3, and channel 4 modulator. The carriers are not modulated to assist in looking at in-band intermodulation. The combined spectrum of these three modulators is shown in Figure 12.



K factor
≈2%
2T Sin^2 Pulse



Envelope Delay
≈0
Modulated 20T Pulse

Figure 11. Video test signal response of modulator–processor (with delay equalization) – demodulator.

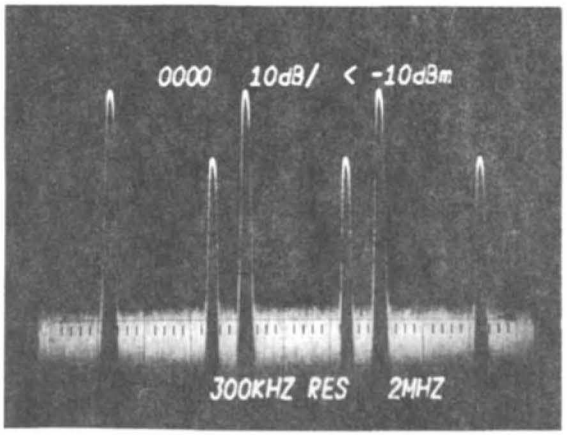
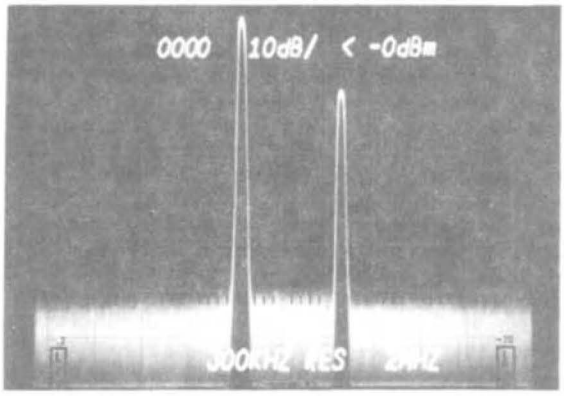
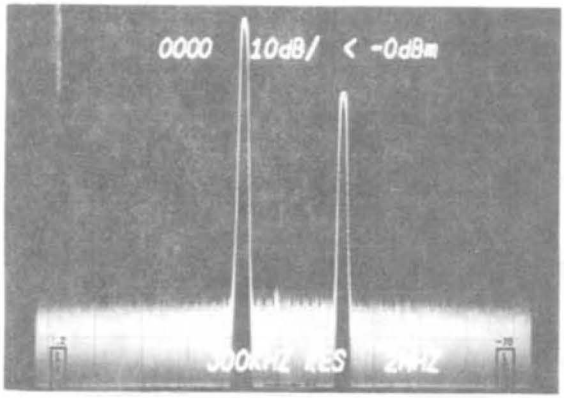


Figure 12. Combined output of Ch 2, Ch 3, and Ch 4 modulator.

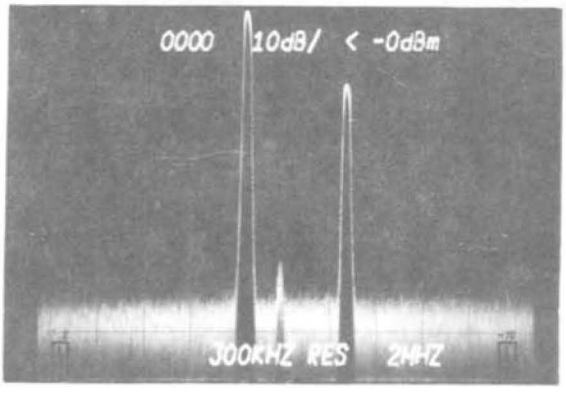
These signals were then fed through a 6150 channel 3–3 processor with the input levels set first at +10 dBmV, then at +20



Input Level
+10 dBmV



Input Level
+20 dBmV



Input Level
+30 dBmV

Figure 13. Output spectrum of 6150 Ch 3 – Ch 3. processor with equal level input signals on Ch 2, Ch 3, and Ch 4.

dBmV, and finally at +30 dBmV. Figure 13 is the output spectrum of the processor for these three levels. Note that with input levels of +30 dBmV, an in-band spurious signal is visible 1.5 MHz above the desired video carrier. Fortunately, this undesired signal is highly dependent upon the input levels and when they are set to +10 dBmV it is well below the noise level. It is a well known fact that due to the delayed AGC, very little improvement is achieved in the output signal to noise ratio by feeding the processor with more than a +10 dBmV. Because of this no loss in output signal to noise ratio must be sacrificed in order to achieve sufficient "linearity" prior to removal of the adjacent channels.

This article has discussed three important requirements for signal processors if they are to function successfully in modern day headend-hub systems. Certainly 60 dB adjacent channel rejection and the capability of handling equal level adjacent channels are a necessity if the processors at the hub site are to operate without external traps and/or filters. Delay equalization, if not a necessity, is certainly desirable, especially in cases where the signal is processed twice. This by no means exhausts the list of desirable and in many cases necessary features for signal processors. Obviously, spurious free outputs from 5 MHz to 300 MHz are required if external filters are to be eliminated. IF switching options, battery power capability, standby carrier modulation capability, phase lock capability are all desirable features. The requirements I discussed were chosen because headend-hub systems emphasized these limitations in first generation solid state signal processors.

[1] Frederick E. Terman, Electronic and Radio Engineering, Fourth Edition, Sec. 11-3, pp. 379-381.

[2] Tektronix, Nomographs for Measuring Relative Delay and Amplitude Using Modulated 20T Pulse for 625/50 Standards.

[3] T. M. Gluyas, Jr., "Television Transmitter Considerations in Color Broadcasting." RCA Review, September 1954, pp. 312-334.