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Full Duplex DOCSIS (FDX) Amplifier Automatic Configuration

A Technical Paper prepared for SCTE by

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1. Introduction

Full Duplex Data-Over-Cable Service Interface Specifications (DOCSIS®)(FDX) technology has been realized in a custom system on a chip (SoC) successfully implemented in an operational FDX remote PHY (R-PHY) node design. A new implementation of this SoC is also being adapted for use in an FDX amplifier utilizing the same echo cancellation technology employed in the node.

FDX amps will begin to replace conventional mid-split amps and will support concurrent bidirectional communication within the same bandwidth. These amps are more complex to configure for FDX operation. Completely new and more complicated procedures for configuring these amplifiers are needed to install these amps. Additionally new procedures to maintain proper operation of these new amplifiers will be needed.

Embedded digital signal processing within DOCSIS 4.0 FDX amplifiers provides the ability to automatically configure the amp for FDX operation, replacing the manual alignment process in conventional amps today. Optimal results for cascades of amps can be obtained resulting in near perfect amp alignment that is otherwise not possible.

The heart of these FDX amps use digital signal processing (DSP) in a custom SoC that digitizes all inbound and outbound signals with flexible processing of the required amplifier gain, equalization, and echo cancellation.

Several test points and a wideband Fast Fourier Transform (FFT) processor for spectrum analysis are included in the SoC in addition to the required DSP for digital filtering, echo cancellation, and FFT signal processing. These digital test points can be processed by the wideband FFT for spectrum analysis. Such processed spectral data can be communicated through an embedded cable modem (eCM) in the SoC, as well as the loading of data as the result of processing this spectrum data for configuring proper amplifier operation. The alignment process for technicians can therefore be simplified through automation via a communication link between the amp and a configuration server using internal amp measurements that are described in this paper.

This paper discusses a method for automatically configuring an FDX amplifier for optimal operation using the spectral analysis capability and DOCSIS communication in the SoC. Additionally, a method for discovering the network topology of the amplifiers in a tree and branch network is derived. Such methodologies can also be used to initially set up and periodically check for continued proper operation of installed and configured amplifiers.

2. FDX Amplifier Design

A functional diagram of an FDX amplifier is shown in Figure 1. This amplifier functionally contains much of a conventional frequency division duplex (FDD) amplifier with the diplex filters replaced by directional couplers or splitters to enable simultaneous bidirectional spectral occupancy in the FDX band. The insertion of a SoC provides echo cancellation of the downstream echo into the upstream signal and DSP features such as digital equalization of upstream and downstream signals. A DOCSIS embedded cable modem (eCM) enables communication between the amp and a central controller (“Amp Central”) to provide network operational parameters and control amplifier setup and determination of network topology of the amplifier cascades within the tree and branch system architecture. The mid-split upstream path is separated via diplex filters and does not pass through the SoC to facilitate network connectivity of the eCM within the SoC.

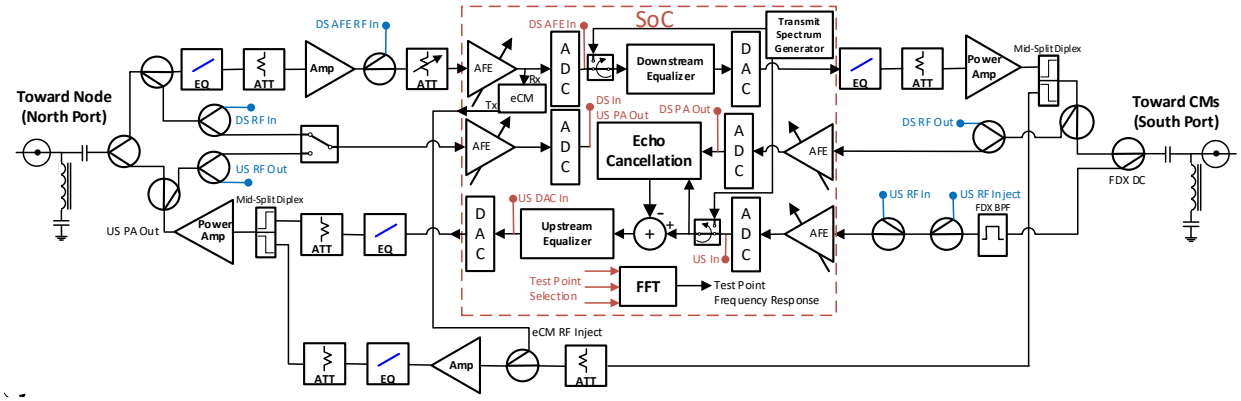


Figure 1 – FDX Amplifier Functional Diagram

An FFT for frequency response (FR) calculations of signal test points is provided within the SoC. Various test points within the SoC are identified in Figure 1. An FFT can be applied to any selected test point to calculate the test point signal FR. Such calculated FRs along with configuration file FRs of the paths between the amp ports and the SoC are used to determine automatic equalization DSP coefficients (in frequency and/or time domain) in the SoC to augment conventional gain and equalization within the amp signal paths.

3. FDX Initial Amplifier Install and Setup

3.1. Define Amp Configuration Files

Configuration file paths #1 through #7 are shown in Figure 2.

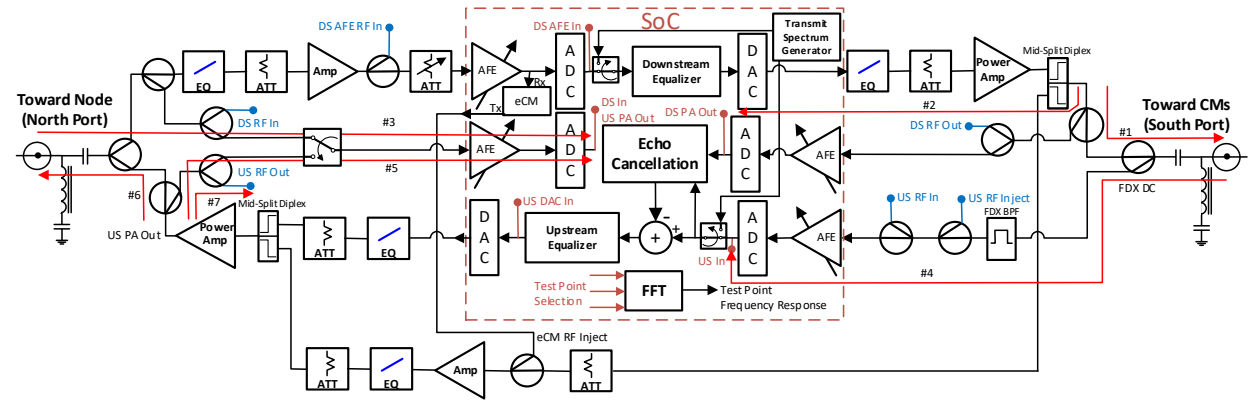


Figure 2 – FDX Amplifier Configuration File Paths

Every configuration file contains an FR (i.e., complex valued scattering parameter s21 with log magnitude < 0 dB) that was measured during the manufacturing process and subsequently stored in the amplifier's memory. By utilizing the configuration files, the levels at the amplifier ports are calculated based on the measurements of the SoC internal test point FR. These calculations, and the resultant calibration of the gains and equalization, both internal and external to the SoC, are discussed in subsequent sections.

3.2. Initial Amp Setup to Enable SoC eCM Activation

3.2.1. Initial Boot-up and Downstream Input Setup

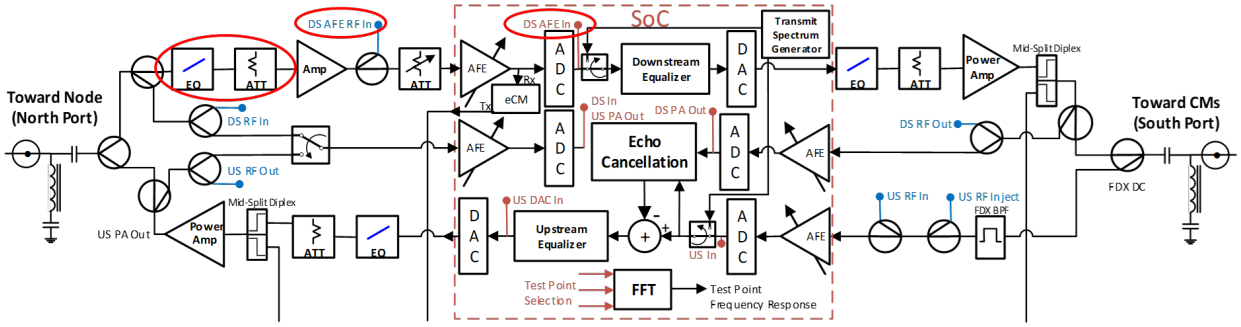


Figure 3 – Initial Boot-up and Downstream Input Setup

Assume that an existing amp is being replaced with the FDX amp shown in Figure 3. The following procedure will setup an initial downstream input to the FDX amp SoC and enable the eCM to establish connectivity with Amp Central as follows:

- Replace the amp housing (new) or RF lid (existing) with the AC power shunts initially removed, then reinstall after the replacement is complete
- Power-up and boot the RF board and SoC module to set the default state for the RF South Port digital-to-analog converter (DAC) attenuator and equalizer (EQ), and the SoC configuration default states for the North Port analog front end (AFE), South Port DAC, North Port DAC, South Port US and DS AFEs
- Set the ADU to manual
- Measure the spectrum and total composite power (TCP) at the **DS AFE RF In** test point with the (measurement) meter tool across test frequencies
- Calculate and set DS input attenuator (ATT) and equalizer (EQ) for approximately a flat level across frequency less than or equal to the TCP limit including the North AFE backoff attenuator (0 dB default) at the **DS AFE RF In** input for the best analog-to-digital converter (ADC) performance
- Measure and adjust the ADU pilot level attenuation in auto mode to match the manual mode

3.2.2. Legacy Upstream Input Setup

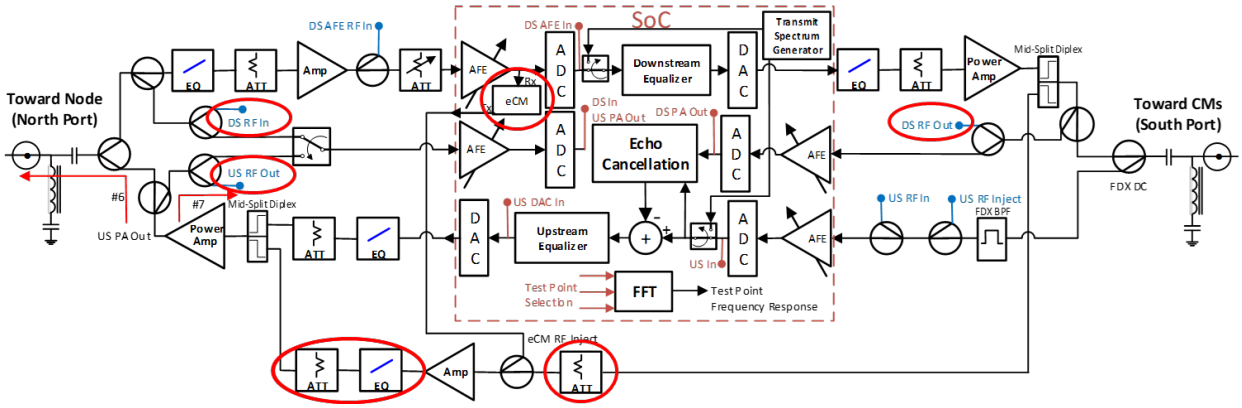


Figure 4 – Legacy Upstream Input Setup

Setup the legacy mid-split upstream path of the FDX amp in Figure 4 as follows:

- Consult the design reference for return input attenuation value
- Set the default state for the legacy US pre-amp input attenuator, US power amp output attenuator, and US output EQ
  - Legacy upstream plug-ins could use previously installed amplifier values initially
- Connect the (measurement) meter tool eCM to the **DS RF In** (CM downstream input) and **DS RF Out** (CM upstream output) test points
- Check the **DS RF Out** test point legacy upstream FR with the (measurement) meter tool with the meter eCM injecting an upstream signal into **DS RF Out** and displaying the upstream spectrum on the meter
- Adjust the US power amp output attenuator and US output EQ to match the upstream FR design reference value at **DS RF Out**
  - **DS RF Out** FR = South Port upstream input FR + Config #1 FR – Config #2 FR[1]
  - Alternatively, define and store a single Config #1-2 FR = Config #1 FR – Config #2 FR

The SoC eCM then locks with a positive status indicator and establishes connectivity to Amp Central. Automatic calculation can proceed with this communication path established. Calculations and results can be handled in Amp Central or CPU processors in the amp or in the SoC (in addition to internal signal test point FFTs).

4. SoC Downstream Gain and Equalization Optimization

4.1. Initial Downstream Output Setup for Mid-Split Operation

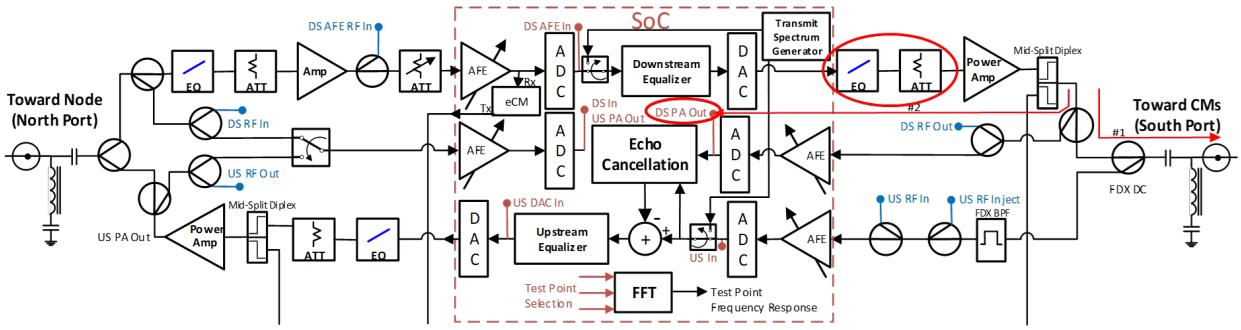


Figure 5 – Initial Downstream Output Setup for Mid-Split Operation

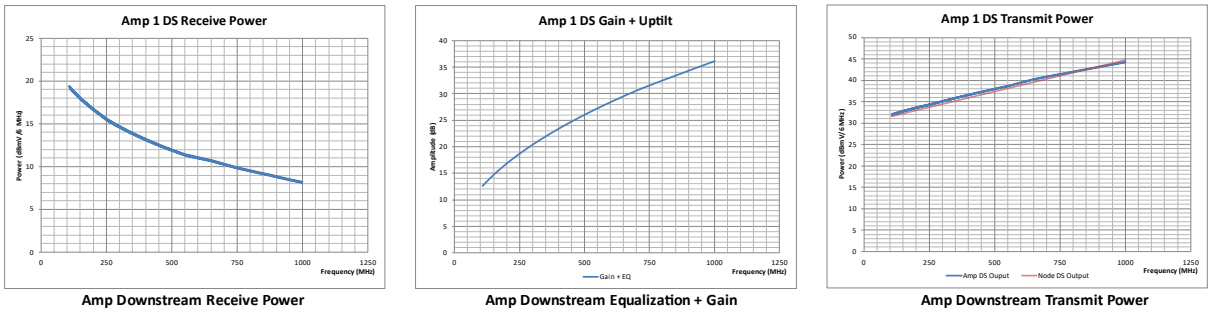
The eCM is online and can query Amp Central for downstream transmit output level and tilt as well as the upstream receive input level. Then, proceed to set the initial gain and tilt in the FDX amp downstream path shown in Figure 5, excluding the SoC, as follows:

- Command the SoC downstream path gain and equalization to 0 dB flat across the downstream band
  - DS DAC input = **DS AFE In** (initially no influence by the SoC digital equalizer, just use conventional or electronic plug-ins)
- Measure the **SoC DS PA out** Frequency Response (FR) downstream output level and tilt values

[1] **DS RF Out** FR + Config #2 FR = South Port upstream input FR + Config #1 FR. So South Port upstream input FR = **DS RF Out** FR + Config #2 FR – Config #1 FR.

- Calculate the South Port-to-**DS PA out** path loss FR = Config #2 FR – Config #1 FR[2]
  - Alternatively, use a single Config #2-1 FR = Config #2 FR – Config #1 FR = –Config #1-2 FR
- Calculate the South Port output FR = **DS PA Out** FR – South Port-to-**DS PA out** path loss FR
- Set the downstream output attenuator and equalizer to approximate the design output level and tilt
- Check the output level and tilt by remeasuring the **DS PA Out** FR and calculating the South Port output FR

The initial setup involves passing the signal through the SoC, which then establishes the downstream connection utilizing conventional attenuators and equalizers, similar to the approach followed in conventional (analog) amplifiers.



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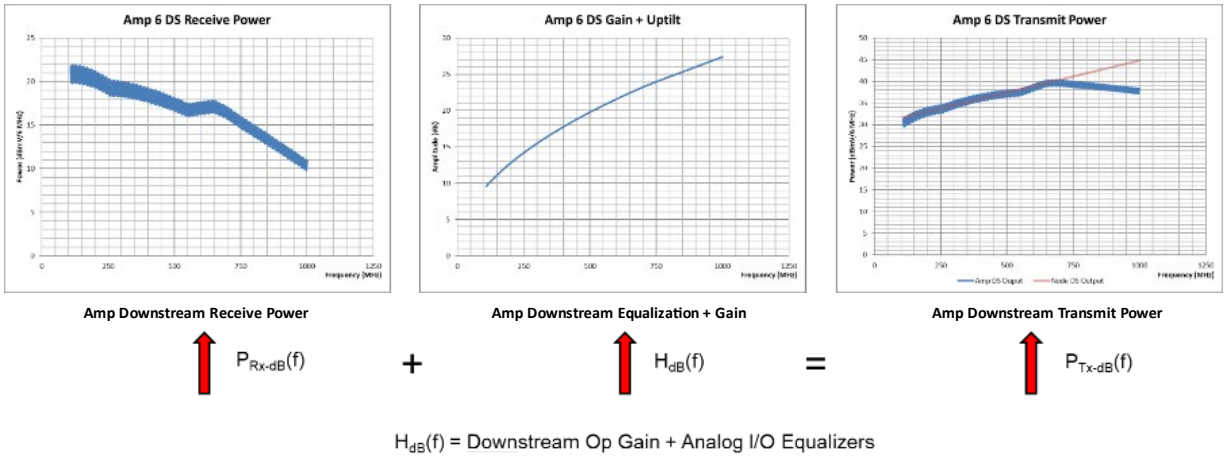


(b)

Figure 6 – Example of Initial Downstream Setup:
(a) Amp 1 Initial Downstream Setup, (b) Amp 6 Initial Downstream Setup

[2] The South Port output FR – Config #1 FR = Diplex common port FR, and the Diplex common port FR + Config #2 FR = **DS PA Out** FR. So the South Port output FR – Config #1 FR = **DS PA Out** FR – Config #2 FR, or the South Port output FR = **DS PA Out** FR – (Config #2 FR – Config #1 FR).

The following network simulations are calculated using the methodology in [1]. As shown in Figure 6, this approximates the design level and tilt design profile and passes any input linear distortion (amplitude variation) to the output signal. The following section removes these artifacts.

4.2. Downstream Output Optimization using SoC Downstream Equalizer

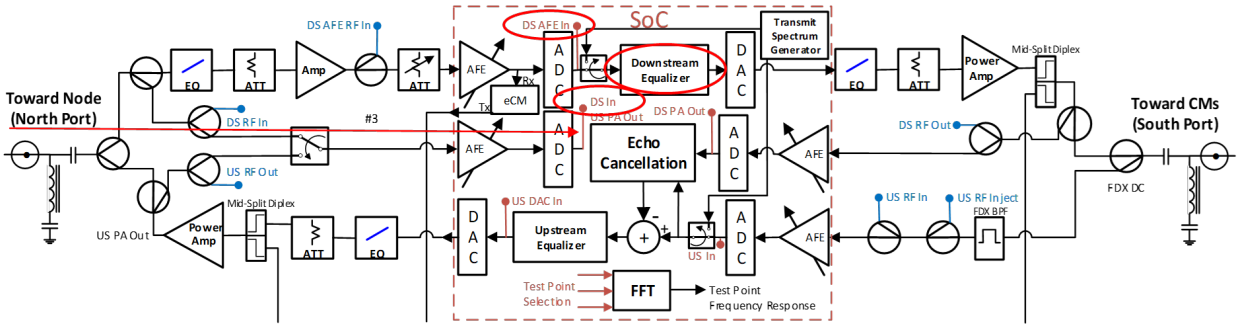


Figure 7 – Downstream Output Optimization using SoC Downstream Equalizer

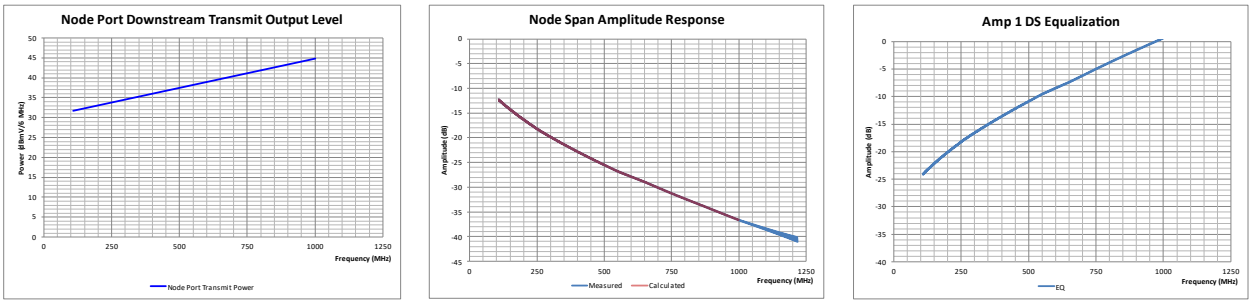
In this section, the design level and tilt design profile are restored and any input linear distortion (amplitude variation) to the output signal is removed as follows:

- Measure the **SoC DS in** FR and **SoC DS AFE in** FR
- Set the North Port-to-**DS in** FR = Config #3 FR
- Calculate the North Port DS input FR = **DS in** FR – North Port-to-**DS in** FR
- Calculate the Inter-Amp Span Loss FR = North Port DS input FR – Node/Amp output design FR
  - Node/Amp output design FR = Node/Amp downstream output design level and tilt FR
- Calculate the North Port-to-**DS AFE in** FR = **DS AFE in** – North Port DS input FR
- Calculate the SoC DS DAC Out-to-South Port FR = **DS AFE in** – South Port output FR
  - SoC Downstream Equalizer = 0 dB in FDX band → DS DAC input = **DS AFE in**
- Calculate DS Equalization + Gain FR = –Inter-Amp Span Loss FR (unity gain)
- Calculate DS Op Gain (> 0 dB) for DS Equalizer FR (≤ 0 dB)
  - DS Op Gain = |DS Equalizer + Gain FR @ maximum DS frequency|
- Calculate DS Equalization FR = –(DS Op Gain + Inter-Amp Span Loss FR)
- DS Equalization FR + DS Op Gain = North Port-to-**DS AFE in** FR + SoC Downstream Equalizer FR + DS DAC input-to-South Port FR
- Set SoC Downstream Equalizer FR = DS Equalization FR + DS Op Gain – North Port-to-**DS AFE in** FR – DS DAC input-to-South Port FR
- FDX downstream path configuration is complete

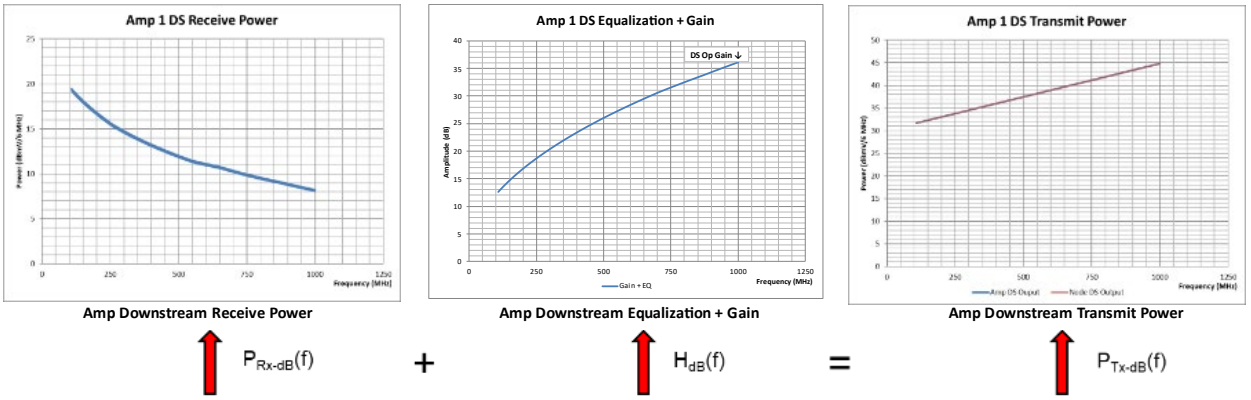
An example depicting the DS Equalization + Gain FR, the Op Gain, and DS Equalization FR calculation steps above that are needed for determining the SoC DS Equalizer FR is shown in Figure 8.
The node transmitted downstream output FR is shown in the left plot of Figure 8a. The amp received downstream input FR is shown in the leftmost plot of Figure 8b. The DS Equalization + Gain FR and DS Op Gain are shown in the center plot of Figure 8b. The output FR (i.e., the level and tilt) matches that of the negative inverse of the inter-amp span loss in the center plot of Figure 8a. The downstream equalization calculation without the op gain is shown in the right plot of Figure 8a. The amp downstream

output transmit FR is shown compared to the node downstream output transmit FR in the right plot of Figure 8b. The downstream output FR (i.e., the level and tilt) matches that of the node with a final 37 dB amp downstream operational gain.

This final setup with activation of the SoC downstream (digital) equalizer and gain setting achieves the design level and tilt design profile and removes any input linear distortion (amplitude variation) to the output signal. Examples demonstrating this result are shown in Section 8 Example Auto Setup of Cascaded FDX Amplifier Networks.



(a)



(b)

Figure 8 – Example of Downstream Output Optimization Using SoC Downstream Equalizer : (a) Node/Amp Downstream Transmit Level, Inter-Amp Span Loss, and Amp Downstream Equalization; (b) Amp Downstrean Receive Level, Amp Downstream Equalization and Op Gain, and Node and Amp Downstream Transmit Levels

5. SoC Upstream Gain and Equalization Optimization

The following sections describe a similar process for the upstream. This is possible because the upstream and downstream signals share the same spectrum and experience equivalent amp span loss from the amp North Port to the Node Port, thanks to the symmetry in path loss between the two directions.

5.1. Initial Upstream Output Setup for FDX Operation

The initial upstream output setup procedure of the FDX amp shown in Figure 9 is described in the following:

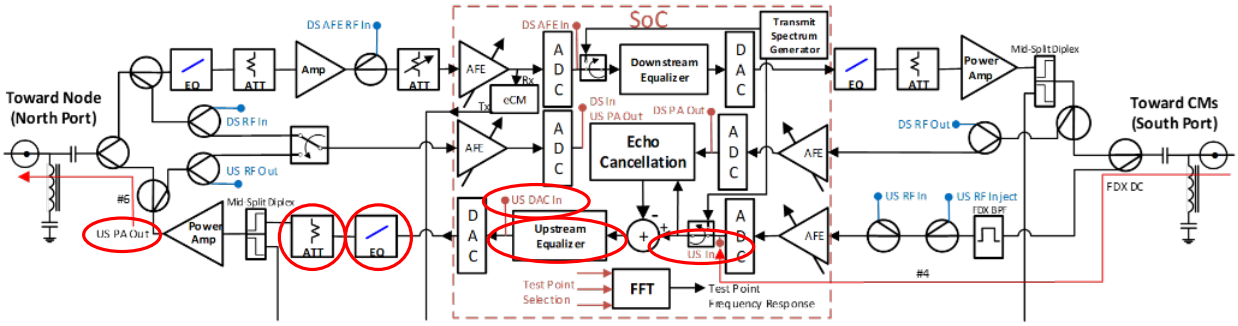
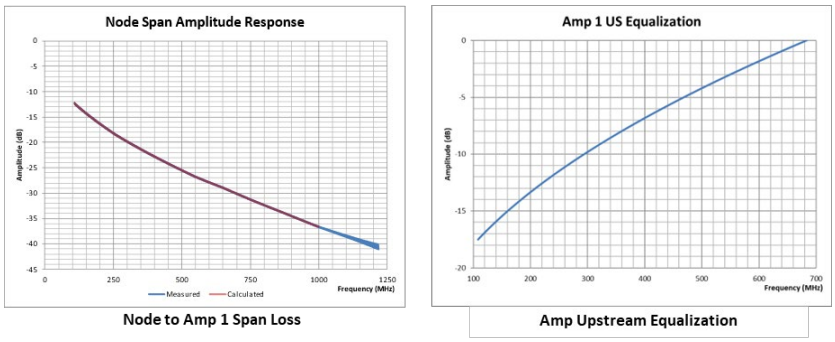


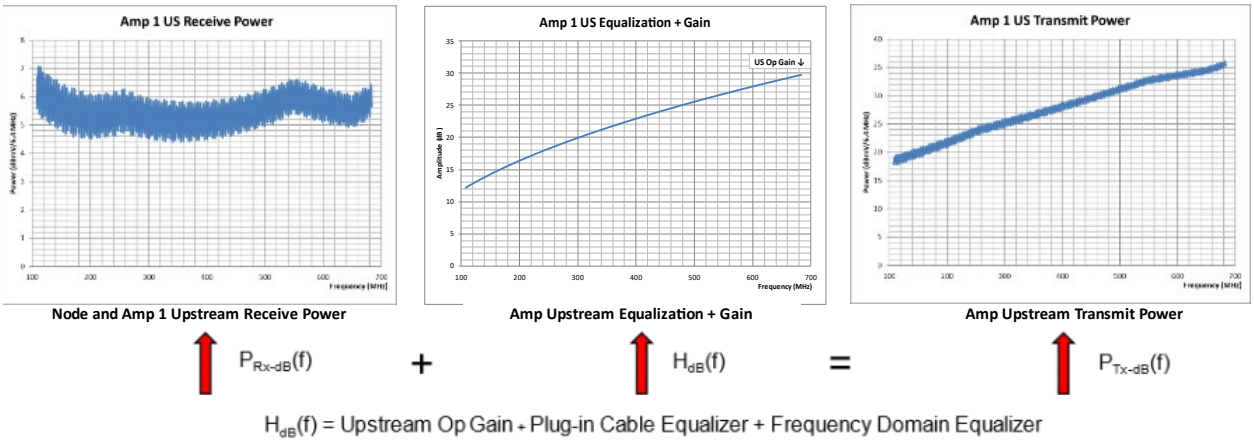
Figure 9 – Initial Upstream Output Setup for FDX Operation

- Command the SoC upstream path gain to 0 dB flat across the upstream band
  - **US in** to **US DAC in**
  - Initially there is no influence by the SoC digital equalizer, just use conventional or electronic plug-ins
- Set the South Port-to-**SoC US in** FR = Config #4 FR
- Set the US PA out-to-North Port FR = Config #6 FR
- Calculate South Port to North Port Amp FR = –Inter-Amp Span Loss FR (symmetric insertion loss)
- Calculate US Equalization + Gain FR = –Inter-Amp Span Loss FR (unity gain)
- Calculate US Op Gain (> 0 dB) for US Equalizer FR (≤ 0 dB)
  - US Op Gain = |US Equalizer + Gain FR @ maximum US frequency|
- Calculate US Equalization FR = –(US Op Gain + Inter-Amp Span Loss FR)
- Calculate US Power Amp Gain = US Op Gain – South Port-to-SoC US in FR – US PA out-to-North Port FR and set upstream output attenuator
- Select plug-in or set electronic US EQ FR ≈ US Equalization FR (match cable EQ uptilt)

An example depicting the US Equalization + Gain FR, the Op Gain, and US Equalization FR calculation steps above that are needed for determining the SoC US Equalizer FR is shown in Figure 10. The US Equalization + Gain FR and US Op Gain are shown in the center plot of Figure 10b. The output FR (i.e., the level and tilt) approximately matches that of the negative inverse of the inter-amp span loss in the center plot of Figure 10a. The upstream equalization calculation without the op gain is shown in the right plot of Figure 10a. The amp upstream output transmit FR is shown in the right plot of Figure 10b. The amp received upstream input FR is shown in the left plot of Figure 10b. The node port upstream input level to be matched at the amp upstream input (South) port is 5 dBmV/6.4 MHz.



(a)



(b)

Figure 10 – Example of Initial Upstream Output Setup for FDX Operation: (a) Inter-Amp Span Loss, and Amp Upstream Equalization; (b) Amp Upstream Receive Level, Amp Upstream Equalization and Op Gain, and Amp Upstream Transmit Level

This approximates the upstream input design level and passes any input linear distortion (amplitude variation) to the output signal. A cable modem transmitting towards the amp south port will transmit with pre-equalization to be received at the node port with a flat level without linear distortion. The upstream input FR (i.e., the level and tilt) approximates that of the node since the amp has not applied upstream equalization in the SoC to reduce the CM linear distortion due to pre-equalization. This is discussed in the next section.

5.2. Upstream Input Optimization using SoC Upstream Equalizer

Completion of the upstream input optimization is accomplished by setting the SoC upstream equalizer to correct the deviation of the US EQ FR from the ideal US Equalization FR calculated in the previous section as follows:

- SoC Upstream Equalizer FR + US EQ FR = US Equalization FR

- Set SoC Upstream Equalizer FR = US Equalization FR – US EQ FR
  - SoC corrects any deviation of US EQ FR from US Equalization FR
- FDX upstream path configuration is complete

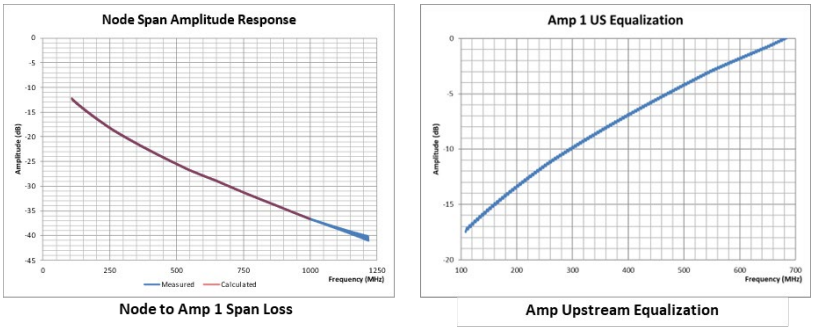
Figure 11 shows the effect of the SoC upstream equalizer on the previous example. The US Equalization + Gain FR and US Op Gain are shown in the center plot of Figure 11b. The output FR (i.e., the level and tilt) now matches that of the negative inverse of the inter-amp span loss in the center plot of Figure 11a. The upstream equalization calculation without the op gain is shown in the right plot of Figure 11a. The amp upstream output transmit FR is shown in the right plot of Figure 11b. The amp received upstream input FR is shown in the left plot of Figure 11b. The node port upstream input level to be matched at the amp upstream input (South) port is 5 dBmV/6.4 MHz.

The final upstream equalization calculation is shown in Figure 11a. The amp upstream input FR is shown in the leftmost plot of Figure 11b. The initial US Equalization + Gain FR is shown in the center plot. The amp upstream output transmit FR is shown in the rightmost plot. The upstream input FR (i.e., the level) is high due to a low initial 0 dB amp gain.

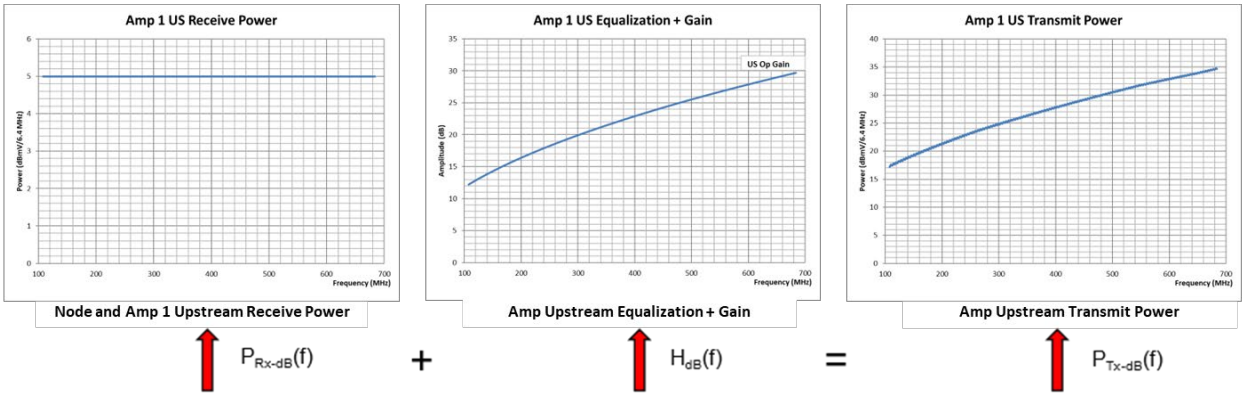
The final upstream equalization calculation is shown in Figure 11b. The final US Equalization + Gain FR is shown in the center plot. The amp upstream output transmit FR is shown in the rightmost plot. The input FR (i.e., the receive level) now matches the node port upstream input level with a final 30 dB amp upstream operational gain.

This final setup with activation of the SoC upstream (digital) equalizer and final gain setting achieves the node upstream input design level and removes any input linear distortion (amplitude variation) to the input signal. Examples demonstrating this result are shown in Section 8 Example Auto Setup of Cascaded FDX Amplifier Networks.

Proceed to the next Section 6 Network Amplifier Topology Discovery after all amps in the node leg have been configured before the final optimization in Section 7 Final Downstream and Upstream Optimization of All Amps.



(a)



(b)

Figure 11 – Example of Upstream Input Optimization Using SoC Upstream Equalizer: (a) Inter-Amp Span Loss, and Amp Upstream Equalization; (b) Amp Upstream Receive Level, Amp Upstream Equalization and Op Gain, and Amp Upstream Transmit Level

6. Network Amplifier Topology Discovery

A functional diagram of an FDX amplifier with topology discovery paths is shown in Figure 12. Using the embedded cable modem in each FDX amplifier, as depicted in Figure 12, the network topology can be determined by transmitting individually, one at a time, in any order, through the mid-split upstream. During each transmission, all amplifiers that detect the signal at the SoC US PA out test point are connected in the upstream path, forming a link between the transmitting amplifier and the node. Note that the transmitting amp will also receive its own injected transmission into the mid-split upstream path.

An example tree and branch network diagram of a cable plant depicting amplifier cascade connectivity is shown in Figure 13. A single port is connected to 25 amplifiers with a maximum cascade depth of 6 (Node + 6). Each amp has a single downstream input (North Port). An amp can have multiple downstream outputs (South Ports), which are also multiple upstream inputs. Splitters/directional couplers can also combine paths that are external to the amplifier port(s) but are considered direct connections to the amplifier. Either a direct or a combined path between amps is a network connection.

Such topology can be represented as a linear graph. Linear graphs are commonly used to describe electrical network topology with associated cut-set (Kirchoff Current Law) or loop-set (Kirchoff Voltage Law) matrices. Network elements (e.g., R, L, and C) are represented as nodes with connections between nodes represented as edges. A non-zero matrix element indicates an edge connection between nodes.

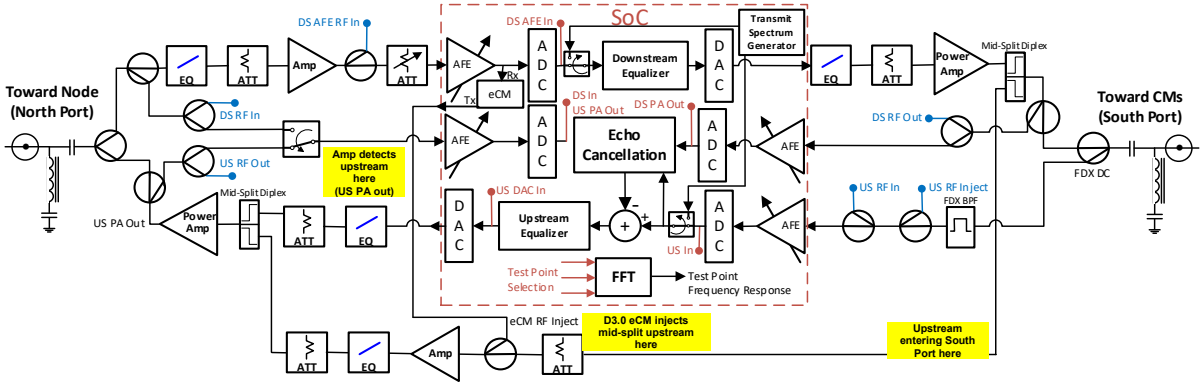


Figure 12 – FDX Amplifier With Topology Discovery Mid-Split Upstream Signal Paths

For determining network topology of amplifier connections, a similar principle can be applied. Each amp in the cable network is a "node", and each input or output connection between amps is an "edge". Network topology is represented as a matrix of unidirectionally edge connected nodes from each end-of-line amplifier toward the FDX node.

A linear graph matrix describing such edge connections of amp nodes between each transmitting amp and all receiving amp nodes in the path toward the cable system fiber node for the network of Figure 13 is shown in Figure 14. A non-zero row element in the matrix denotes an edge connecting amp in the path between, and including, the transmitting amp and the root amp connected directly to the fiber node. Each "1" cell represents a mid-split upstream transmission in a row amp that is received by that column amp. For example, node row 14 indicated that this amp transmission can be heard by receiving column node amps 13 and 1 (as well as itself).

Some properties of this matrix can be used to determine the network topology of all amp cascades from an end-of-line amp to the fiber node. The row sum is equal to the number of amps that received the transmission of that row amp and represents the cascade depth of the transmitting amp in a network branch. The column sum is equal to the number of amps whose transmissions were received by that column amp (including itself). For example:

- The column of amp 14 did not receive any other amp transmission except itself (a single "1" in column 14) and is therefore at the end-of-line of a network branch.
- The column of amp 13 received a transmission only from itself and amp 14 (rows 13 and 14).
- The column of amp 1 received transmissions from every amp in the network, i.e., it is the root amp of the network tree (amp cascade level 1) connected to the fiber node.

A branch starts at an end-of-line amp where the # of edges in the column sum is equal to 1, i.e., there are no amps downstream of this amp. Each amp in the branch (cascade) from that end-of-line amp to the root amp (connected to the node) has a non-zero cell in the row of that end-of-line amp. To determine network topology, sort each non-zero cell amp in the end-of-line amp row in decreasing order (from the end-of-line amp to the root amp) according to the row sum (amp level) of each non-zero amp in the row.

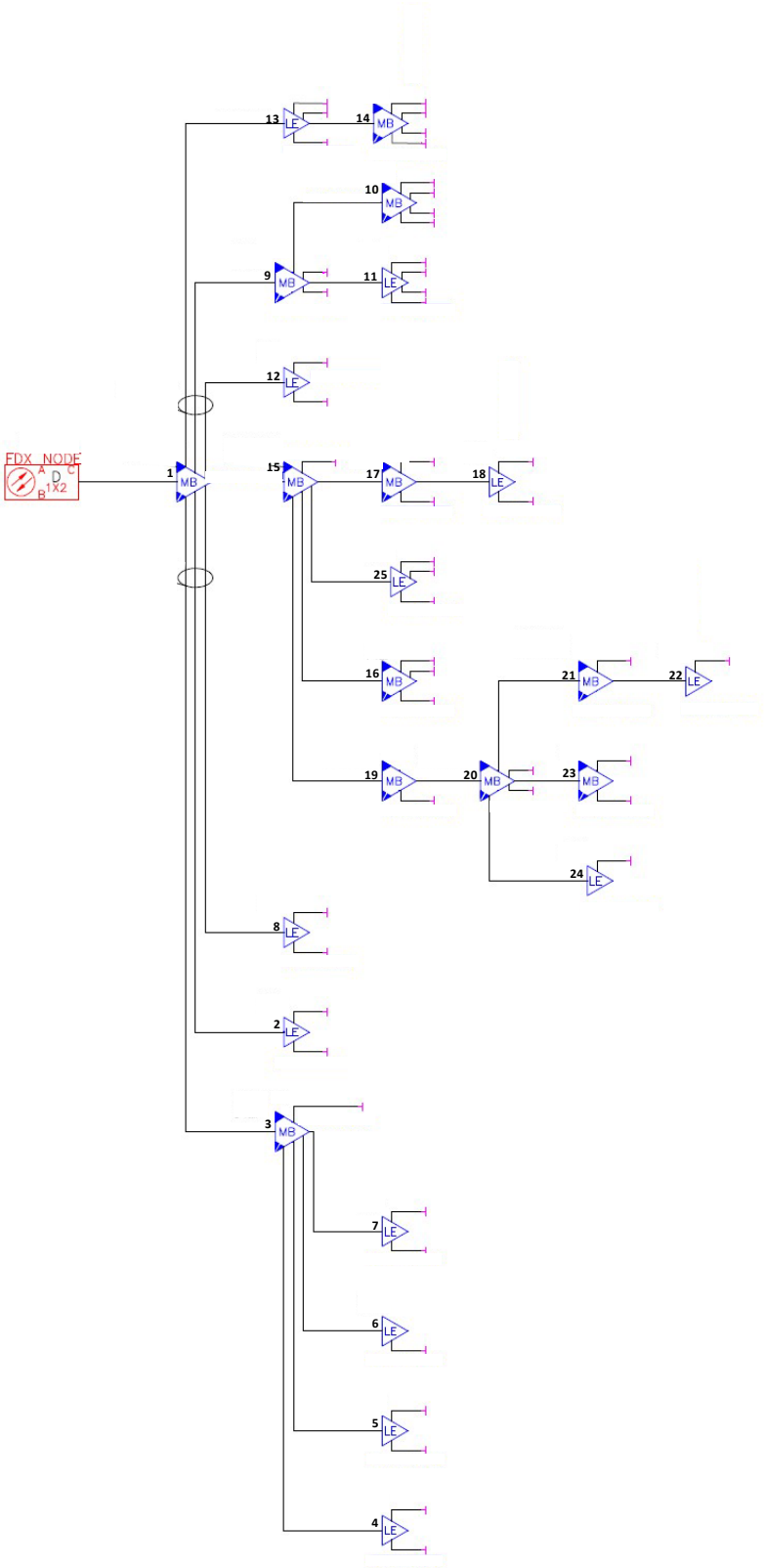


Figure 13 – Example Tree and Branch Cable Network

For example:

- amp 14 column total (# of edges) = 1 and is at a branch end-of-line
- row 14 connects with edges to columns 13 and 1
- row 14 sum (amp cascade level) = 3
- row 13 sum (amp cascade level) = 2
- row 1 sum (amp cascade level) = 1
- Therefore, the path of this branch from the end-of-line (amp level 3) to the root (amp level 1) is 14, 13, 1 as shown in Table 1

	# of edges	25	1	5	1	1	1	1	1	3	1	1	1	2	1	11	1	2	1	6	5	2	1	1	1	1
Amp Level		Receive																								
	nodes	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
1	Transmit 1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	2	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	3	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	4	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	5	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	6	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	7	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	8	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	9	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	10	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	11	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	12	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
2	13	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
3	14	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
2	15	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
3	16	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
3	17	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
4	18	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0
3	19	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
4	20	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0
5	21	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0
6	22	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0	0
5	23	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	1	0	0
5	24	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	0
3	25	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

Figure 14 – Matrix Describing the Tree and Branch Cable Network of Figure 13

Table 1 – Network Topology Describing the Tree and Branch Cable Network of Figure 13

Network Topology for Node +6

End of Line Amps:		2		4	5	6	7	8		10	11	12		14		16		18				22	23	24	25
Toward Node ↓		1		3	3	3	3	1		9	9	1		13		15		17				21	20	20	15
				1	1	1	1			1	1			1		1		15				20	19	19	1
																		1				19	15	15	
																						15	1	1	
																						1			

7. Final Downstream and Upstream Optimization of All Amps

After completing Network Amplifier Topology Discovery, repeat previous Downstream and Upstream Optimizations successively from ALL level 1 to level x amps. Each amp at level n initially relies on the downstream output profile of amp n-1 matching that of the node. This is only true if FDX amps are configured successively from the node toward the end of line. Configuring amps in any other order will measure conventional amplifier downstream output profiles which may differ from that of the node resulting in some deviation from the node downstream output level profile. A second pass configuration in order from the node toward the end of line (N+1 to N+x) corrects any such deviations resulting in each amplifier downstream output matching that of the node.

Each amplifier upstream gain and FR can now be precisely adjusted by using a transmit spectrum generator signal from each end-of-line amplifier as follows:

- Check Amp/Node upstream receive level with SoC Transmit Spectrum Generator (Figure 15)
  - Query Amp Central for Node/Amp Port FDX upstream input level (constant value over frequency)
  - Set Transmit Spectrum Generator level successively at each end of line amp = FDX upstream input level + <South Port-to-SoC US in FR>

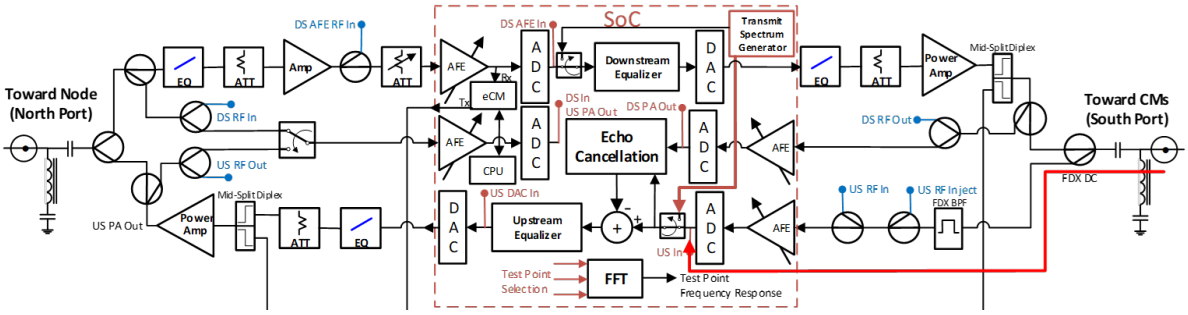


Figure 15 – Set SoC Transmit Spectrum Generator to Check Amp/Node Receive Level

- Check upstream alignment (and redo if needed) from the end of line toward the node
  - Back to front from amp cascade level x to 1 for a N + x system after network amp topology discovery
  - Turn on the Transmit Spectrum Generator signal in the FDX upstream band on the end of line amp x
  - Successively check each amp upstream receive level at amp x-1,x-2,…,1 at SoC US in test point in each cascade path from each end of line amp x
  - Check for each amp received upstream input level at SoC US in FR = Node/Amp Port FDX upstream input level FR, where the Node/Amp Port FDX upstream input level FR should be a constant value over frequency[3]

8. Example Auto Setup of Cascaded FDX Amplifier Networks

The methodology described for automatic configuration of FDX amplifiers, designed with DSP in the SoC shown in Figure 1, is applied to two examples of amplifier cascades within cable systems. Firstly, to a suburban system of single-family units with distributed taps separated by about 100 feet with amps

[3] Since the Transmit Signal Generator injects a constant level across the FDX band at the SoC US In test point, the Config #4 FR from the South Port to the SoC US In test point is not shaping the test signal FR. So the upstream input of the receiving amps South Port north of the transmitting amp will be the Node/Amp Port FDX upstream input level FR - Config #4 FR. Then the successive SoC US In test point level FRs will be the Node/Amp Port FDX upstream input FR - Config #4 FR + Config #4 FR = Node/Amp Port FDX upstream input FR.

spaced about 800 feet in a 6-amp cascade. Secondly, to an urban multiple dwelling unit, multi-story building with 4 or more back-to-back tap clusters separated by about 45 feet with 8 taps per amplifier at spacing of about 50 feet for each group of 6 floors.

These two types of systems have significantly different frequency response characteristics that present different challenges to amplifier setup and equalization due to the different mix of cable lengths and tap spacing. Nevertheless, it will be demonstrated that the aforementioned procedures can achieve nearly identical input and output levels across the cascade of amplifiers in a uniform manner, while significantly reducing the accumulation of linear distortion that is typically observed in conventional amplifier cascades.

8.1. Single Family Unit (SFU) Model of a Node + 6 Amp Cascade

An example of a Node + 6 SFU system is shown in Figure 16. The node port input/output and echo interference levels, upstream received signal-to-noise ratio (SNR), and resultant bit-loading is shown in Figure 17.

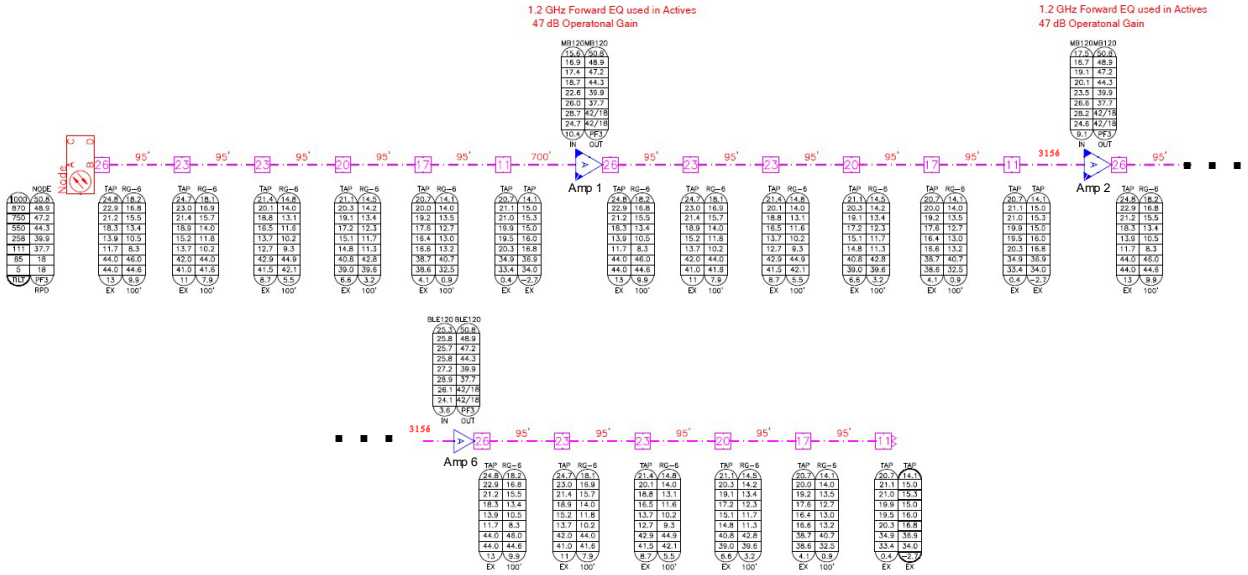
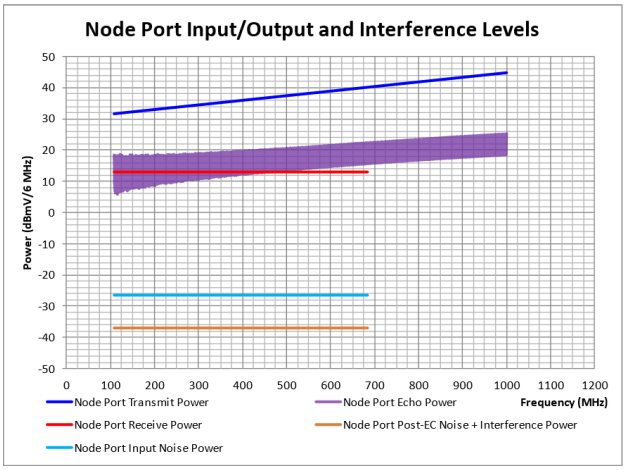
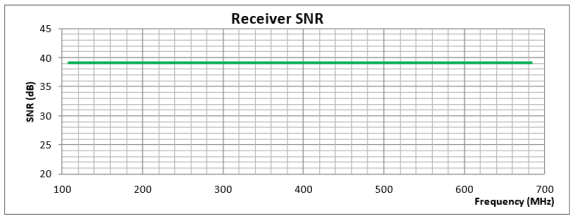


Figure 16 – Example Single Family Unit (SFU) Model for a Node + 6 Amp Cascade

The procedure of Section 4.1 for initial downstream setup for mid-split operation of the amplifiers was applied to Amp 1 of the SFU system of Figure 16. This initially set up the attenuators and equalizers with the SoC passthrough of the downstream signal. The result in Figure 18 for the Amp 1 downstream gain, plus uptilt on the downstream received input, yields the downstream transmitted output shown. Note that the amp output slightly deviates from the node transmitted signal frequency response.

Next, the procedure of Section 4.2 for the final optimized downstream setup of the amplifiers using the digital equalizer in the SoC was applied. The result in Figure 19 for the Amp 1 optimized downstream gain, plus uptilt on the downstream received input, yields the downstream transmitted output shown. Note that the amp output deviation from the node transmitted signal frequency response has been eliminated by the SoC digital equalizer action.





Node and Amp Upstream Input Level: 13 dBmV/6.4 MHz

3.1 Spec	3.1 PMA
Average Bit-Loading Post-EC Echo + D4.0 US Rx + CNR 108 - 684 MHz	Average Bit-Loading Post-EC Echo + D3.1 US Rx + CNR 108 - 684 MHz
9 bits/subc	11 bits/subc

Figure 17 – SFU Node Port Input/Output and Echo Interference Levels

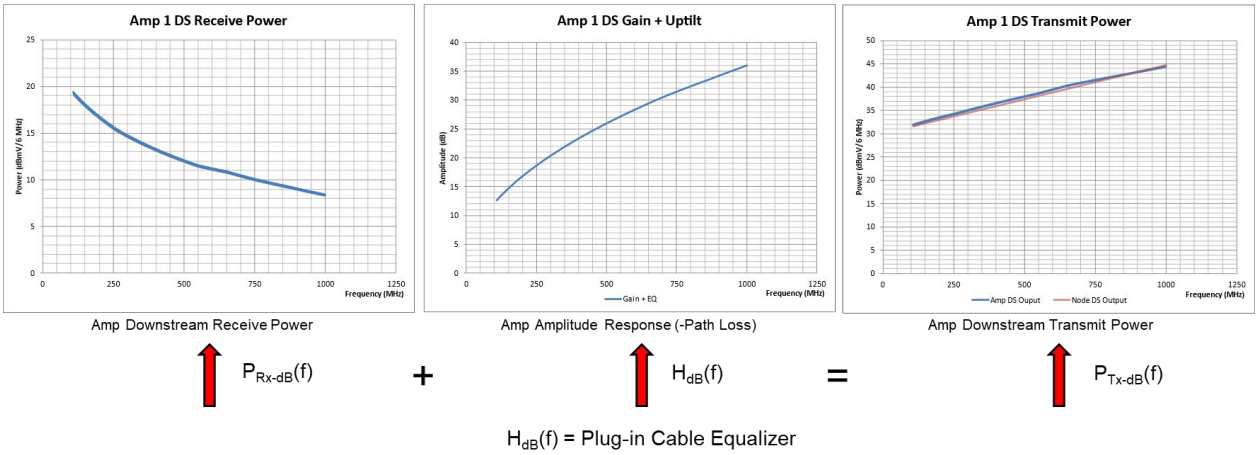


Figure 18 – SFU Amp 1 Initial Downstream Setup

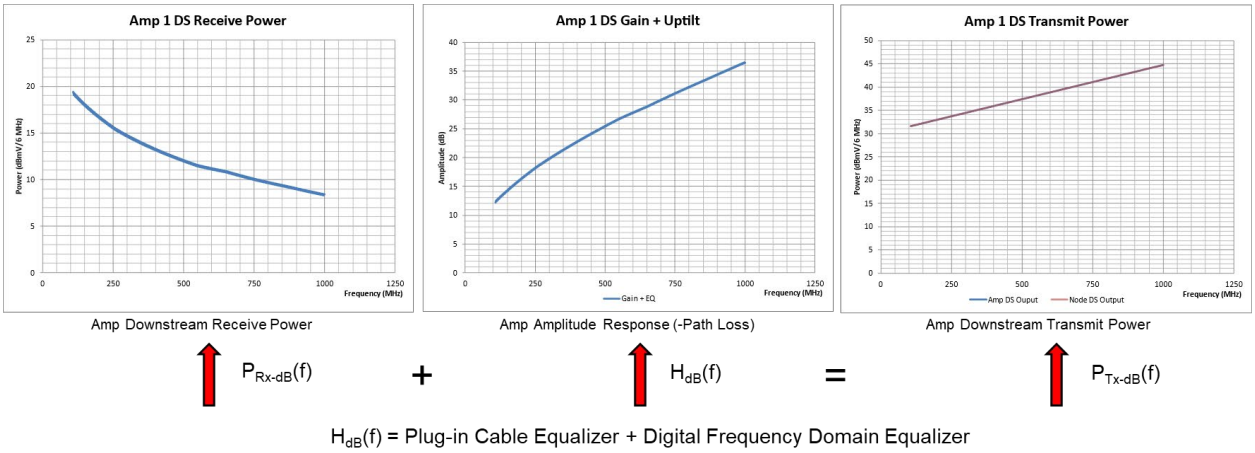


Figure 19 – SFU Amp 1 Final Optimized Downstream Setup

The procedure of Section 4.1 for initial downstream setup for mid-split operation of the amplifiers was applied to Amp 6 of the SFU system of Figure 16. This initially set up the attenuators and equalizers with the SoC passthrough of the downstream signal. The result in Figure 20 for the Amp 6 downstream gain, plus uptilt on the downstream received input, yields the downstream transmitted output shown. Note that the amp output significantly deviates from the node transmitted signal frequency response. High frequency roll-off and linear distortion (amplitude ripple) due to signal reflections increases as the downstream signal traverses through the amp cascade.

Next, the procedure of Section 4.2 for final optimized downstream setup of the amplifiers using the digital equalizer in the SoC was applied. The result in Figure 21 for the Amp 6 optimized downstream gain plus uptilt on the downstream received input yields the downstream transmitted output shown. Note that the amp output deviation from the node transmitted signal frequency response has been eliminated by the SoC digital equalizer action. This is true for each amp in the cascade.

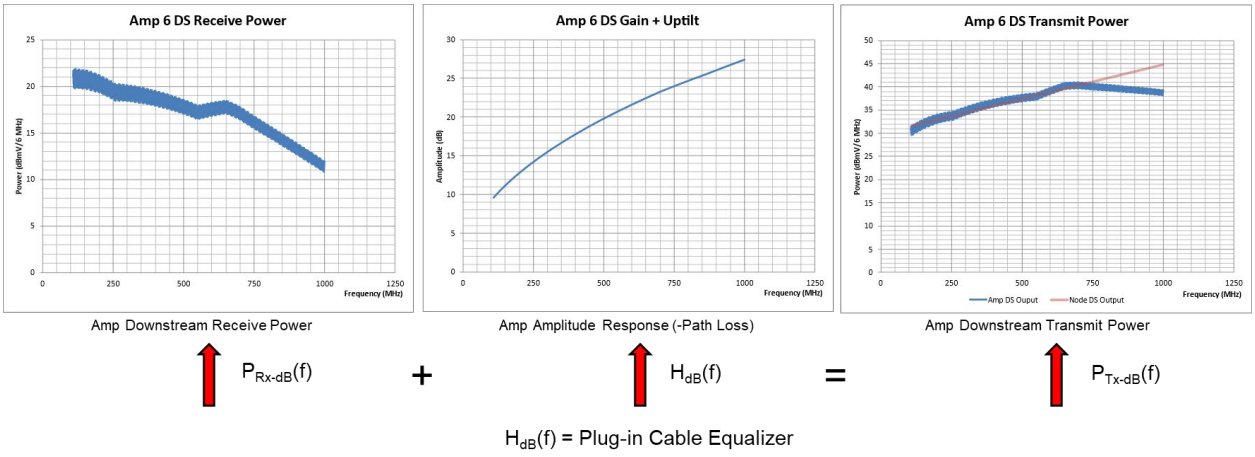


Figure 20 – SFU Amp 6 Initial Downstream Setup

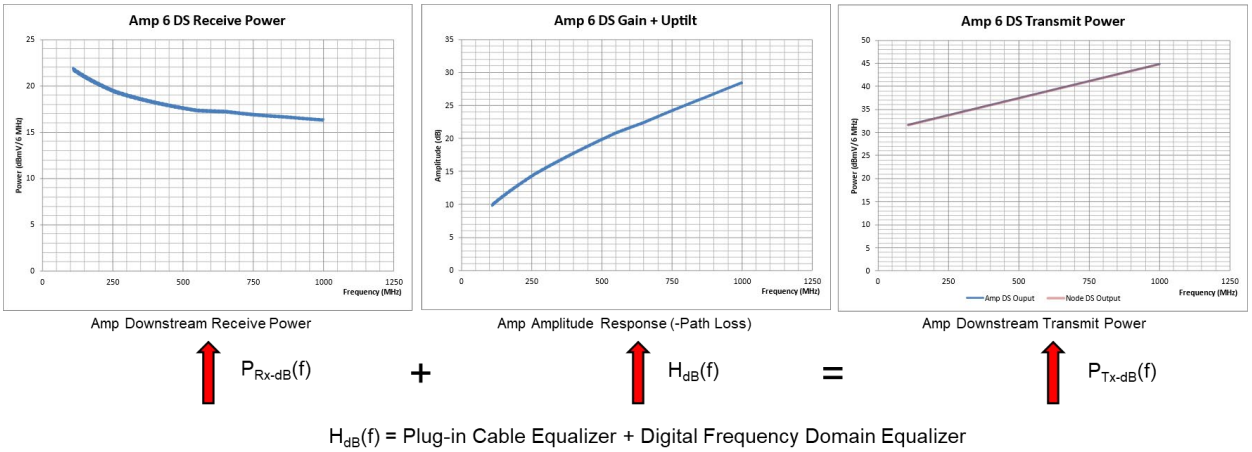


Figure 21 – SFU Amp 6 Final Optimized Downstream Setup

A similar procedure of Section 5.1 for initial upstream setup for FDX operation of the amplifiers was applied to Amp 1 of the SFU system of Figure 16. This initially set up the attenuators and equalizers with the SoC passthrough of the upstream signal. Note that in the upstream direction, Amp 1 is at the end of

the upstream signal cascade. Hence, this amp will have the maximum level deviation and linear distortion in the upstream. The result in Figure 22 for the Amp 1 upstream gain, plus uptilt on the upstream received input, yields the upstream transmitted output shown. Note that the amp input significantly deviates from the node received signal frequency response (flat level). Linear distortion (amplitude ripple) due to signal reflections increases as the upstream signal traverses through the amp cascade.

Next, the procedure of Section 5.2 for the final optimized upstream setup of the amplifiers using the digital equalizer in the SoC was applied. The result in Figure 23 for the Amp 1 optimized upstream gain, plus uptilt on the upstream received input, yields the upstream transmitted output shown. Note that the amp input deviation from the node received signal frequency response (flat level) has been eliminated by the SoC digital equalizer action. This is true for each amp in the cascade.

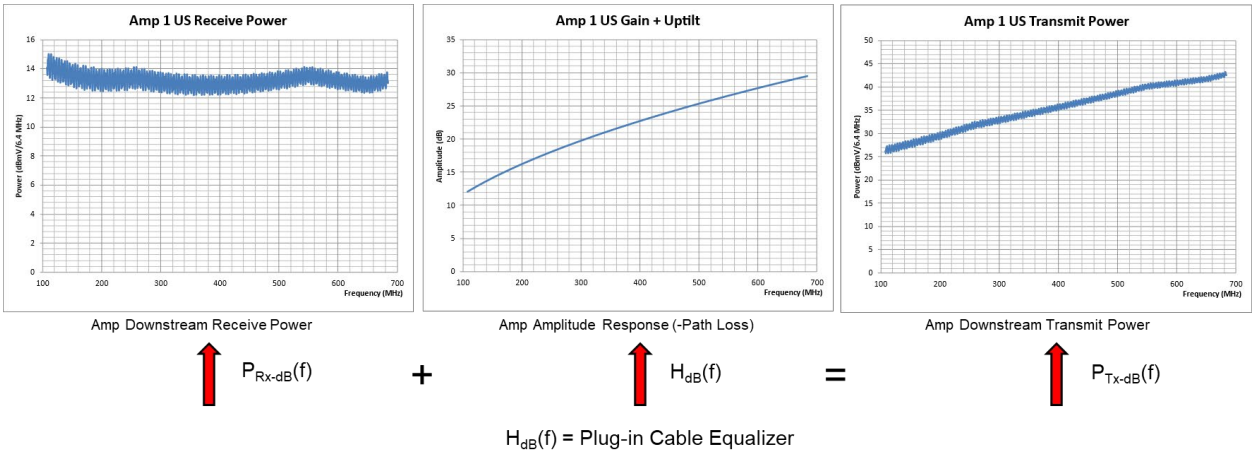


Figure 22 – SFU Amp 1 Initial Upstream Setup

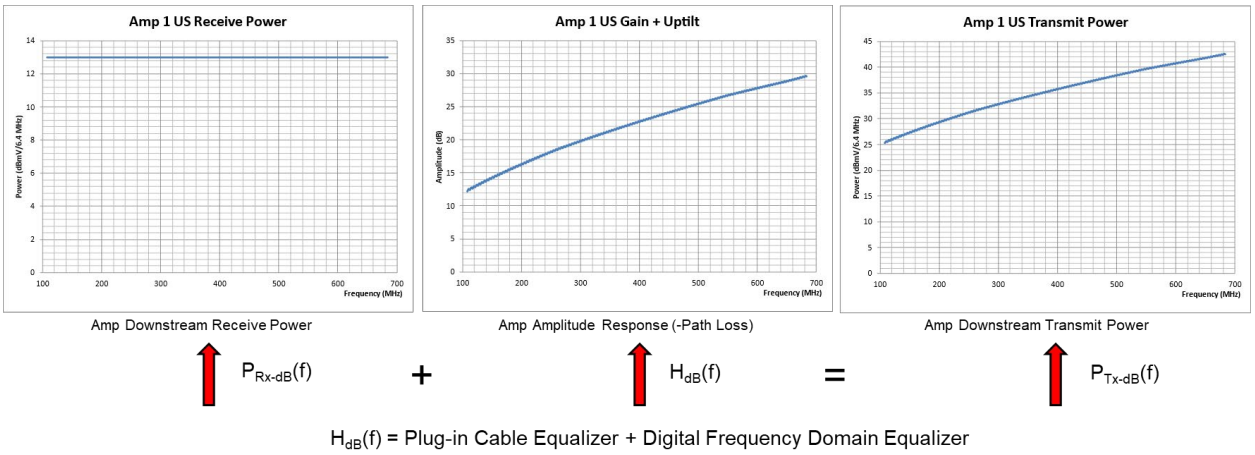


Figure 23 – SFU Amp 1 Final Optimized Upstream Setup

8.2. Multiple Dwelling Unit (MDU) Model of a Node + 6 Amp Cascade

An example of a Node + 6 MDU system is shown in Figure 24.

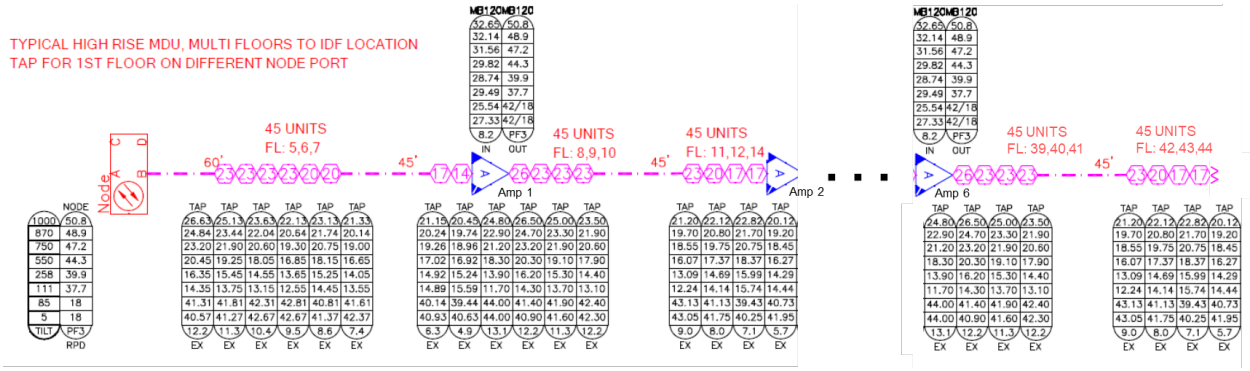


Figure 24 – Example Multiple Dwelling Unit (MDU) Model for a Node + 6 Amp Cascade

The node port input/output and echo interference levels, the upstream received SNR, and resultant bit-loading are shown in Figure 25.

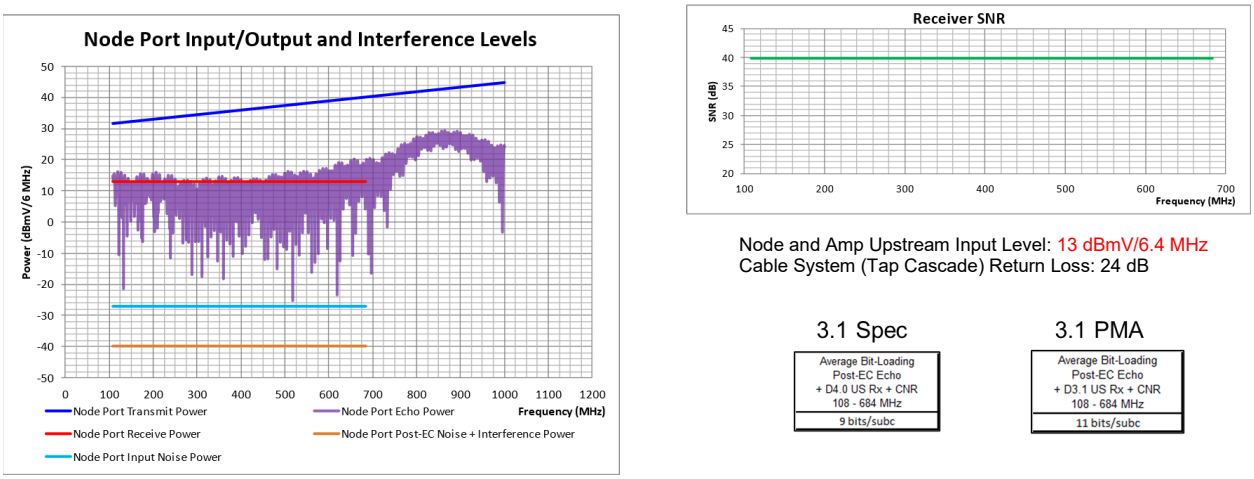


Figure 25 – MDU Node Port Input/Output and Echo Interference Levels

The procedure outlined in Section 4.1, which pertains to the initial downstream setup for mid-split operation of the amplifiers, was implemented specifically on Amp 1 of the MDU system depicted in Figure 24. This initially set up the attenuators and equalizers with the SoC passthrough of the downstream signal. The result in Figure 26 for the Amp 1 downstream gain, plus uptilt on the downstream received input, yields the downstream transmitted output shown. Note that the amp output slightly deviates from the node transmitted signal frequency response.

Next, the procedure of Section 4.2 for final optimized downstream setup of the amplifiers using the digital equalizer in the SoC was applied. The result in Figure 27 for the Amp 1 optimized downstream gain, plus uptilt on the downstream received, input yields the downstream transmitted output shown. Note that the amp output deviation from the node transmitted signal frequency response has been eliminated by the SoC digital equalizer action.

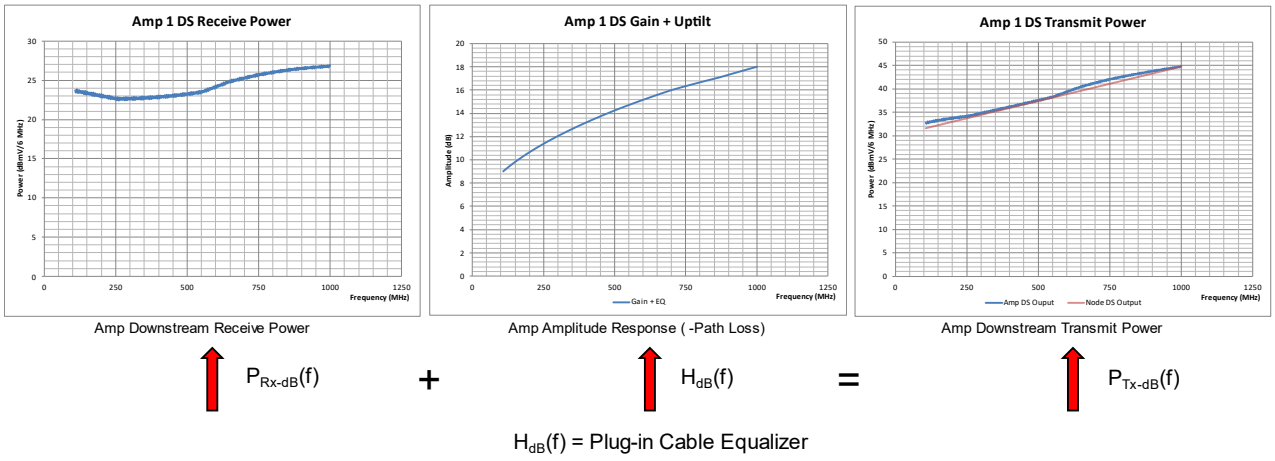


Figure 26 – MDU Amp 1 Initial Downstream Setup

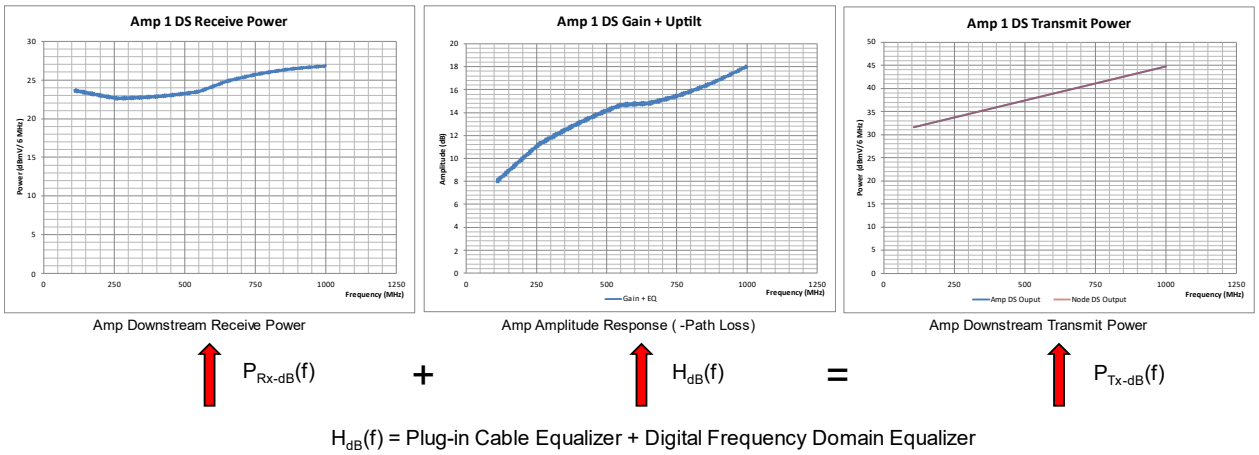


Figure 27 – MDU Amp 1 Final Optimized Downstream Setup

The procedure of Section 4.1 for initial downstream setup for mid-split operation of the amplifiers was applied to Amp 6 of the MDU system of Figure 24. This initially set up the attenuators and equalizers with the SoC passthrough of the downstream signal. The result in Figure 28 for the Amp 6 downstream gain, plus uptilt on the downstream received input, yields the downstream transmitted output shown. Note that the amp output significantly deviates from the node transmitted signal frequency response. High frequency roll-off and linear distortion (amplitude ripple) due to signal reflections increases as the downstream signal traverses through the amp cascade.

Next, the procedure of Section 4.2 for final optimized downstream setup of the amplifiers using the digital equalizer in the SoC was applied. The result in Figure 29 for the Amp 6 optimized downstream gain, plus uptilt on the downstream received input, yields the downstream transmitted output shown. Note that the amp output deviation from the node transmitted signal frequency response has been eliminated by the SoC digital equalizer action. This is true for each amp in the cascade.

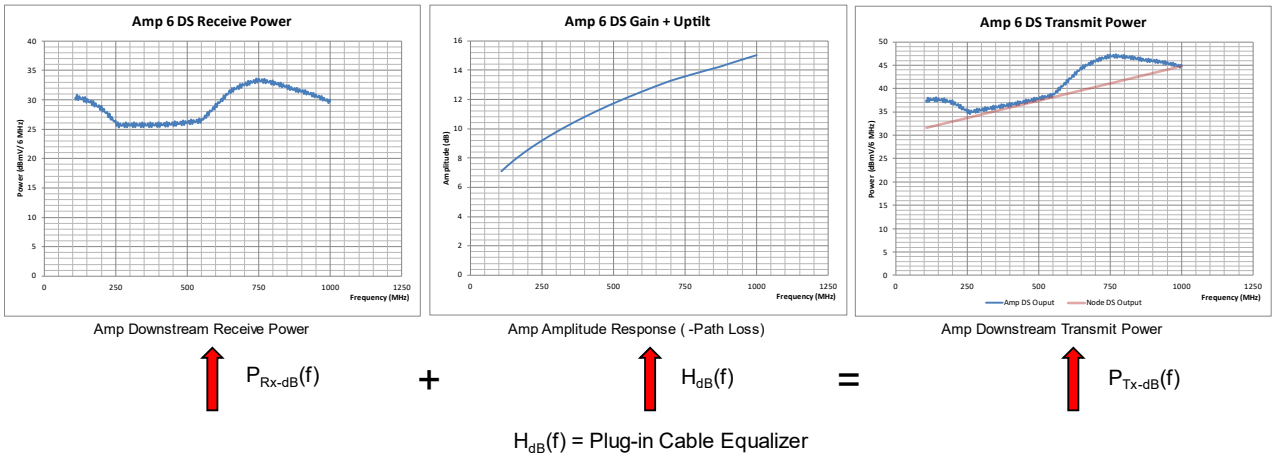


Figure 28 – MDU Amp 6 Initial Downstream Setup

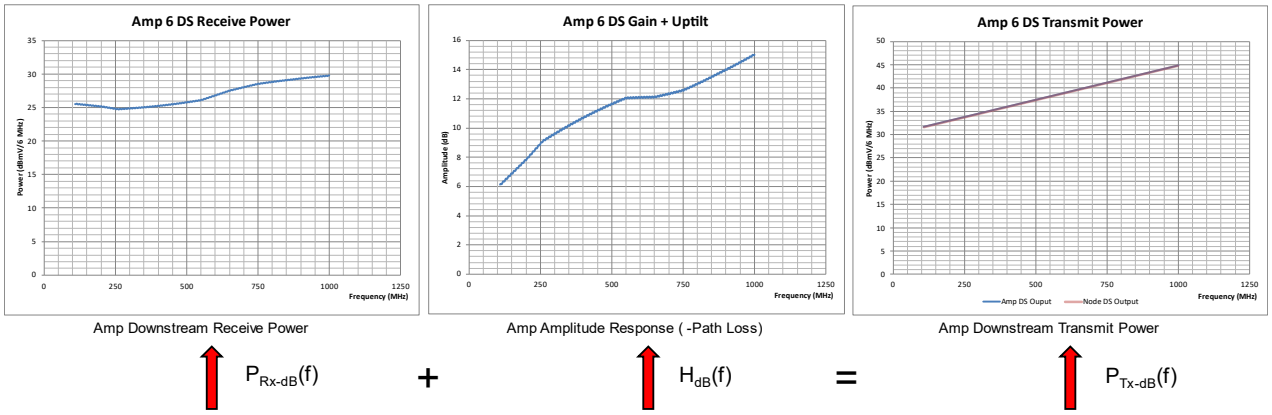


Figure 29 – MDU Amp 6 Final Optimized Downstream Setup

A similar procedure of Section 5.1 for initial upstream setup for FDX operation of the amplifiers was applied to Amp 1 of the MDU system of Figure 24. This initially set up the attenuators and equalizers with the SoC passthrough of the upstream signal. Note that in the upstream direction, Amp 1 is at the end of the upstream signal cascade. Hence, this amp will have the maximum level deviation and linear distortion in the upstream. The result in Figure 30 for the Amp 1 upstream gain, plus uptilt on the upstream received input, yields the upstream transmitted output shown. Note that the amp input significantly deviates from the node received signal frequency response (flat level). Linear distortion (amplitude ripple) due to signal reflections increases as the upstream signal traverses through the amp cascade.

Next, the procedure of Section 5.2 for final optimized upstream setup of the amplifiers using the digital equalizer in the SoC was applied. The result in Figure 31 for the Amp 1 optimized upstream gain, plus uptilt on the upstream received input, yields the upstream transmitted output shown. Note that the amp input deviation from the node received signal frequency response (flat level) has been eliminated by the SoC digital equalizer action. This is true for each amp in the cascade.

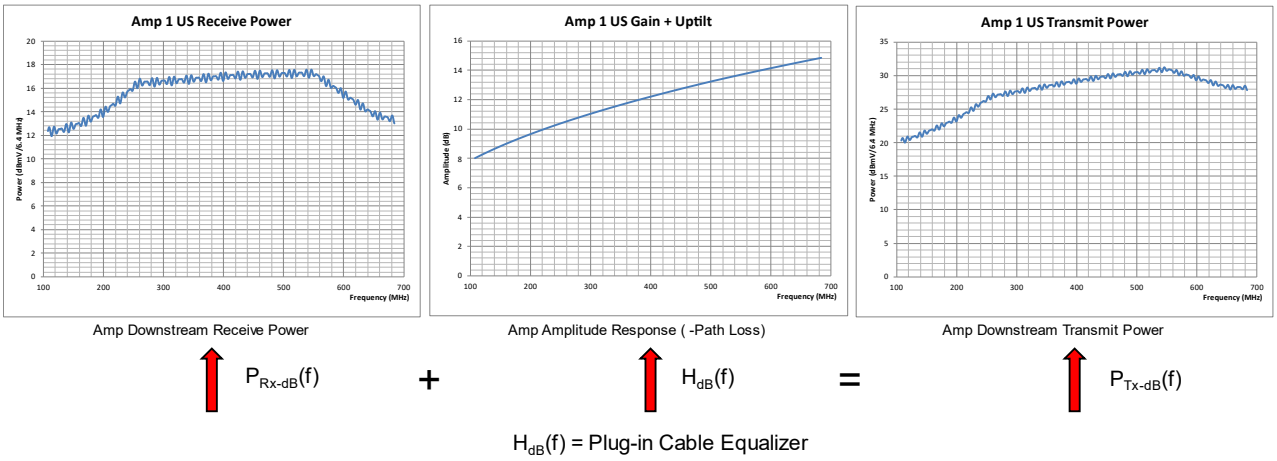


Figure 30 – MDU Amp 1 Initial Upstream Setup

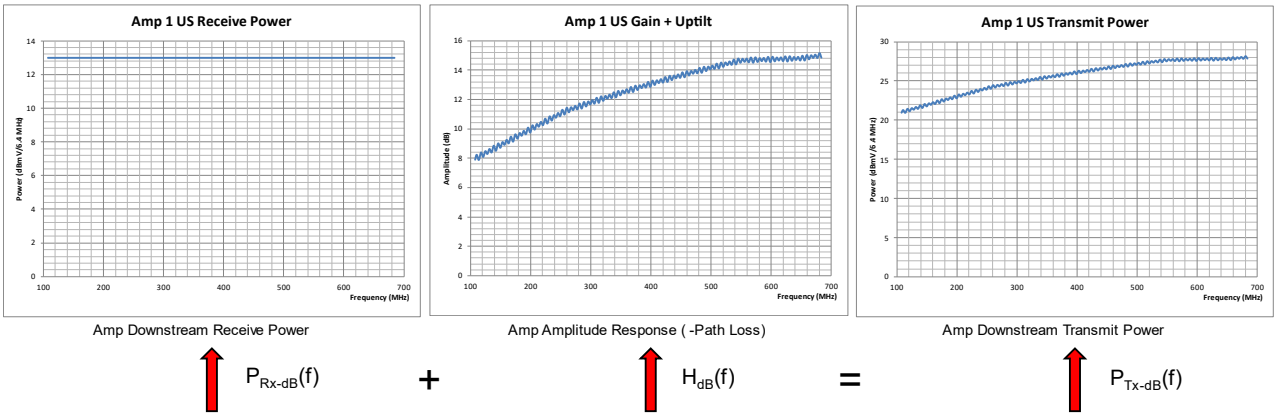


Figure 31 – MDU Amp 1 Final Optimized Upstream Setup

9. Conclusion

Optimized amplifier gain and digital equalization demonstrate superior signal regeneration compared to analog plug-in cable equalizers. ADC, DAC, and FFT processing of signals at input and output test point interfaces included in the DOCSIS 4.0 FDX Smart Amplifier SoC allow frequency domain calculation of amplifier gain and DSP-based equalization.

A multiple step algorithm for automatically configuring FDX amplifier downstream and upstream signals was described, and the resulting performance demonstrated. Optimized digital equalization can restore node output transmission levels, tilt, and input receive levels in cascaded FDX amplifiers. Both example networks discussed demonstrate optimized digital equalization that can restore node transmission levels, tilt, and input receive level in cascaded FDX amplifiers.

A method was described for determining network amp topology using a linear graph matrix with elements determined by mid-split upstream transmission and reception of amp embedded cable modems. This method determines the amp cascade sequence order that could be used to order the automatic amp

configuration process from the node to the end-of-line amp. Such methodologies can also be used to initially set up and periodically check for continued proper operation of installed and configured amplifiers.

Abbreviations

ADC	analog-to-digital converter
ADU	automatic drive unit
AFE	analog front end
DAC	digital-to-analog converter
dB	decibel
dBmV	decibel millivolt
DOCSIS	Data-Over-Cable Service Interface Specifications
DS	downstream
DSP	digital signal processing
eCM	embedded cable modem
EQ	equalizer
FDD	frequency division duplex
FDX	full duplex DOCSIS
FFT	Fast Fourier Transform
FR	frequency response
MDU	multiple dwelling unit
MHz	megahertz
N+x	node plus x amplifiers
PA	power amp
R-PHY	remote PHY
SCTE	Society of Cable Telecommunications Engineers
SFU	single family unit
SNR	signal-to-noise ratio
SoC	system on a chip
TCP	total composite power
US	upstream

Bibliography & References

[1] R.S. Prodan, *Full Duplex DOCSIS PHY Layer Design and Analysis for the Fiber Deep Architecture*, SCTE 2017 Cable-Tec Expo

