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Best Practices for DOCSIS 3.1 Phase Noise Design in the Remote PHY Node

A Technical Paper Prepared for SCTE/ISBE by

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Introduction

This paper presents a best practice for DOCSIS 3.1 phase noise design related to lower cost and higher phase noise performance in remote PHY node/shelf products. The following figure shows a remote PHY device (RPD) block diagram, which is applicable to a remote PHY node or remote PHY shelf.

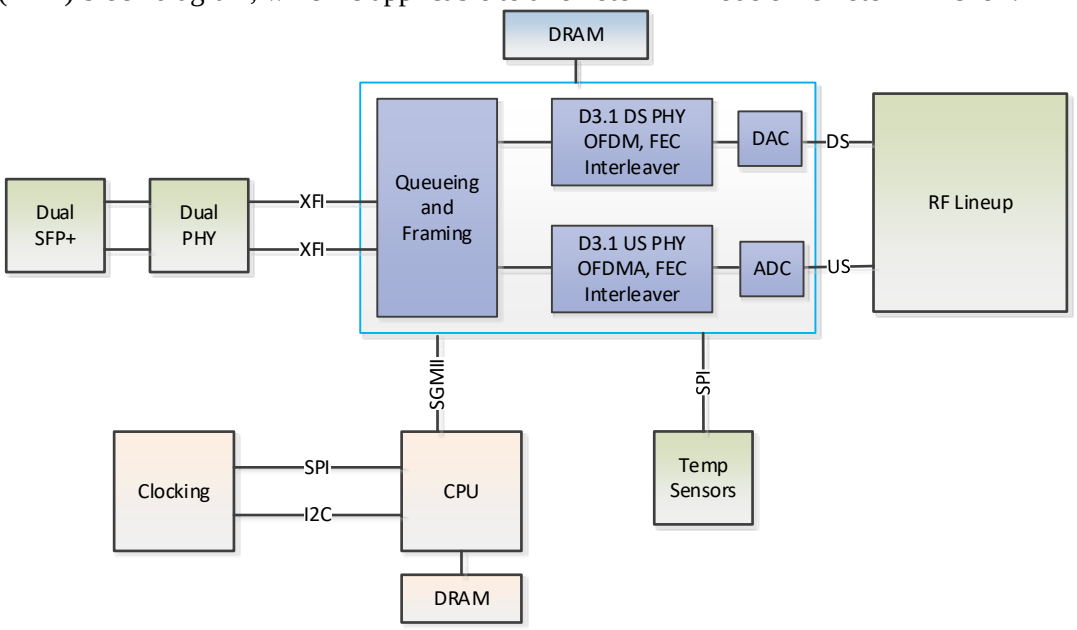


Figure 1 - Remote PHY Device Block Diagram

Clocking

There are two main clock domains in the RPD:

- DOCSIS system clock domain: This is the main data path clock. When the RPD is working in synced clock mode, this clock needs to be synchronized with the CCAP core data clock by R-DTI/IEEE 1588. When the RPD is working in timing re-stamping mode, this clock domain would base on the RPD local TCXO clock source. The DOCSIS timing is based on this clock domain. All of the 10 gigabit Ethernet (GE) interface reference clocks, PHY3.0/3.1 DOCSIS clock (204.8 MHz) are in this clock domain and clock margin is not supported.
- Local system clock domain: local CPU/CPLD/CPU_DDR/FPGA_DDR/PCIe/GE/SGMII clocks need to sync with the DOCSIS clock; those clocks would come from one local 25 MHz TCXO.

Figure 2 shows the RPD clock block diagram.

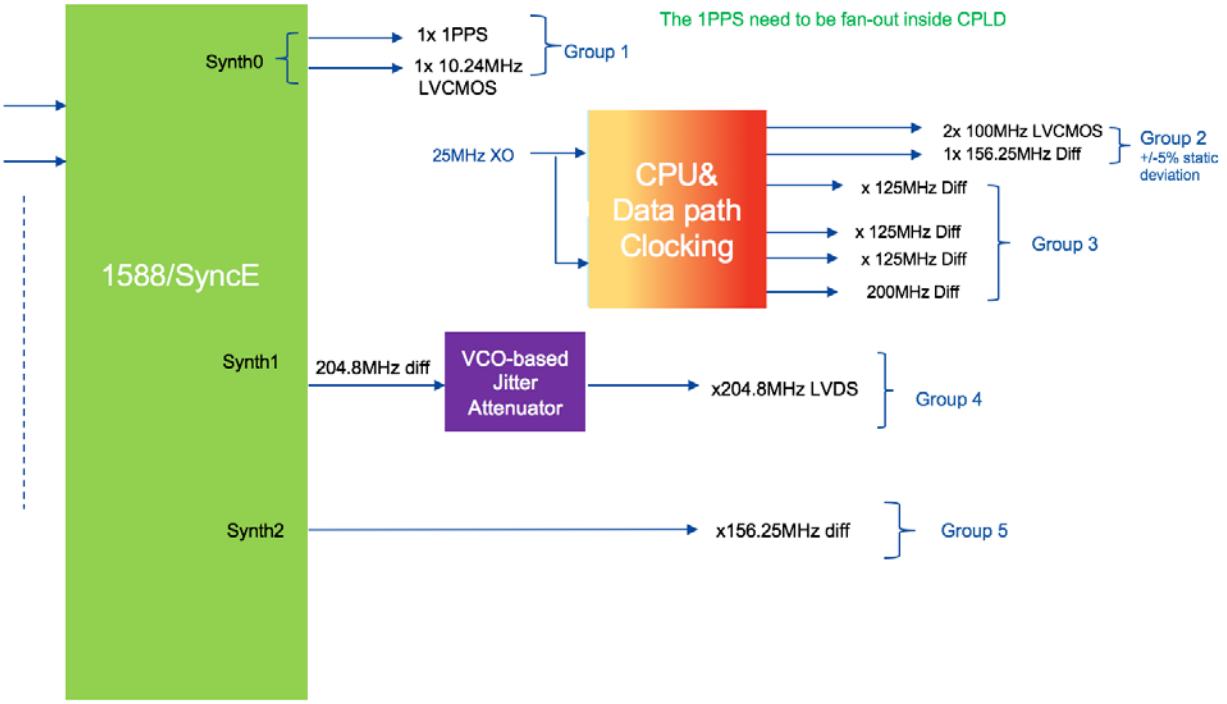


Figure 2 - Clocking block diagram

- ## PHY3.1 Phase Noise Requirement

A clean clock is a necessity when working with high performance D/A or A/D-converters in the remote PHY node/shelf product. For DOCSIS applications, the clock noise requirement is driven by DRFI phase noise requirements as well as the noise and spurious requirements as stated in Table 1.

Table 1 - PHY3.1 phase noise requirement

Phase noise, double sided maximum, Full power CW signal 1002 MHz or lower	1 kHz - 10 kHz: -48 dBc 10 kHz - 100 kHz: -56 dBc 100 kHz - 1 MHz: -60 dBc 1 MHz - 10 MHz: -54 dBc 10 MHz - 100 MHz: -60 dBc
Full power 192 MHz OFDM channel block with 6 MHz in center as Internal Exclusion subband + 0 dBc CW in center, with block not extending beyond 1002 MHz [CW not processed via FFT]	1 kHz - 10 kHz: -48 dBc 10 kHz - 100 kHz: -56 dBc
Full power 192 MHz OFDM channel block with 24 MHz in center as Internal Exclusion subband + 0 dBc CW in center, with block not extending beyond 1002 MHz [CW not processed via FFT]	100 kHz - 1 MHz: -60 dBc
Full power 192 MHz OFDM channel block with 30 MHz in center as Internal Exclusion subband + 7 dBc CW in center, with block not extending beyond 1002 MHz [CW not processed via FFT]	1 MHz - 10 MHz: -53 dBc
Adjacent channel spurious signals and noise	Fc+/-3.75-9 MHz -62 dBc
All other channels spurious signals and noise	47 MHz to 1218 MHz -73 dBc

The "all other channels" specification in Table 1 sets the limit on the wideband noise floor. Hence for wideband noise, the requirement at the DAC output is -73 dBc within a 6 MHz bandwidth, which translates to -141 dBc/Hz. When referenced to the total signal power, this number remains constant as the number of channels is increased.

Assume that the DAC is operated at an update rate of 4 gigasamples per second (GSps); a SNR over Nyquist of 48 dB is required.

- ## Wideband Jitter Requirement

It is well known that the signal to noise ratio of a DAC converting a single tone is

$$SNR[dB] = 20 \cdot \log\left(\frac{1}{2\pi f_c \sigma_t}\right)$$

where f_C is the signal frequency and σ_t is the RMS jitter.

For a finite bandwidth, random, stationary signal with bandwidth fb, it can be shown that the SNR out of the DAC, due to clock noise will be equal to

$$SNR[dB] = 20 \cdot \log\left(\frac{\sqrt{12}}{2\pi\sigma_\tau \cdot \sqrt{f_b^2 + 12 f_c^2}}\right)$$

Using the previous, and assuming that the jitter is caused by white noise and is translated to white noise in the Nyquist bandwidth, noise density can be expressed as

$$N[dBc/Hz] = -20 \cdot \log\left(\frac{\sqrt{12}}{2\pi\sigma_\tau \cdot \sqrt{f_b^2 + 12 f_c^2}}\right) - 10 \cdot \log(f_{DAC}/2)$$

Given that the SNR applies to the Nyquist bandwidth, it follows that noise density will decrease by 3 dB as the clock rate is doubled, assuming that the amount of jitter remains constant.

The maximum allowable jitter to achieve a given noise density is calculated as:

$$\sigma_t = \sqrt{10^{N/10} \cdot f_{DAC}/2 \cdot \frac{3}{\pi^2 \cdot (f_b^2 + 12 f_c^2)}}$$

Assume a signal frequency of fc = 1 GHz, an update rate fDAC = 4 GSps. The maximum noise density for DRFI is -141 dBc. Assume 10 dB margin to this specification to account for sinc attenuation (approx. 1 dB for MAX5882), additional noise sources and margin to the specification, you find the maximum jitter σ_t = 0.2 ps.

• DOCSIS PHY3.1 Chip Phase Noise Requirement

Table 2 shows an example from silicon PHY3.1 chip vendor for phase noise requirement.

Table 2 - DOCSIS3.1 PHY chip phase noise requirement

Reference clock Phase noise (SSB)	@1 kHz	-116 dBc/Hz
	@10 kHz	-134 dBc/Hz
	@100 kHz	**-143 dBc/Hz**
	@1 MHz	-144 dBc/Hz
	>10 MHz	-150 dBc/Hz
Ref. Clock jitter	Integrated, 1 kHz to 20 MHz	225 fs, RMS
	Integrated, 100 Hz to 20 MHz	275 fs, RMS

100 kHz spot phase noise specification derived from the downstream worst-case frequency band [100 kHz to 1 MHz] phase noise specification = -60 dBc.

There are multiple clock solution designs for RPDs.

Table 3 - RF Clock Design Options

Key chip	Key Design	Solution
LMK04828	Jitter Cleaner Single PLL mode with external VCXO 204.8 MHz clock output	Solution 1: VCXO-Based Jitter Cleaner Dual PLL Design
LMK04616	20.48 MHz input, Dual PLL mode (1st stage 122.88 MHz VCXO + 2nd stage internal VCO) 204.8 MHz clock output	
HMC7044	20.48 MHz input, Dual PLL mode (1st stage 122.88 MHz VCXO + 2nd stage internal VCO) 204.8 MHz clock output	
ADF4002	Frequency synthesizer with external VCXO 204.8 MHz clock output	Solution 2: Frequency synthesizer + VCXO

Solution 1: VCXO-Based Jitter Cleaner Design

PHY3.1 silicon vendor has strict requirement on the 204.8 MHz clock for ADC/DAC and 156.25 MHz clock for 10 GE interface.

The IEEE 1588 clock recovery from DPLL has high phase noise and high spurs, so a jitter cleaner device is needed for “cleaning” the 1588 clock.

- **Jitter Cleaner**

Traditionally, the RPD will use a jitter cleaned chip with an external 204.8 MHz VCXO.
There would be two PLL loops, PLL1 uses an external VCXO and loop bandwidth to provide low jitter clean clock, and PLL2 would be used for frequency generation. See Figure 3.

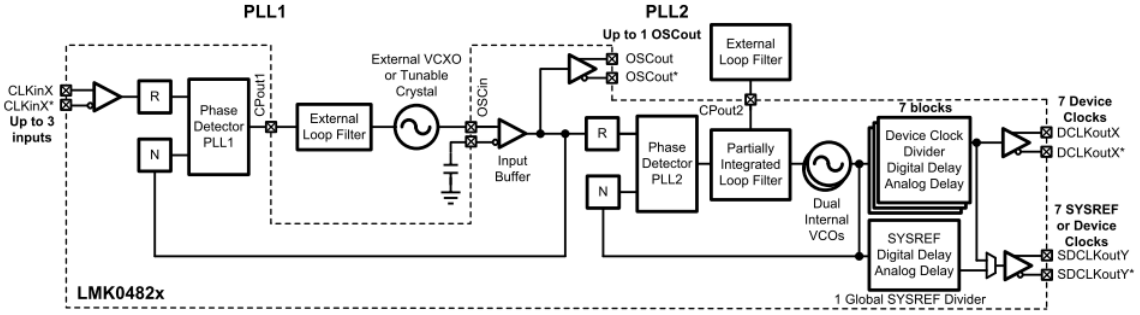


Figure 3 - VCXO-Based Jitter Cleaner Block Diagram

The dual loop PLL architecture of the LMK04828 provides the lowest jitter performance over a wide range of output frequencies and phase noise integration bandwidths. The first stage PLL (PLL1) is driven

by an external reference clock and uses an external VCXO or tunable crystal to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2).

PLL1 uses a narrow loop bandwidth (typically 10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This "cleaned" reference clock provides the reference input to PLL2.

Ultra-low jitter is achieved by allowing the external VCXO or crystal's phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies.

On the RPD, PLL2 is not used and is bypassed. Only PLL1 is used to generate the 204.8 MHz clock for the PHY3.1 silicon chip

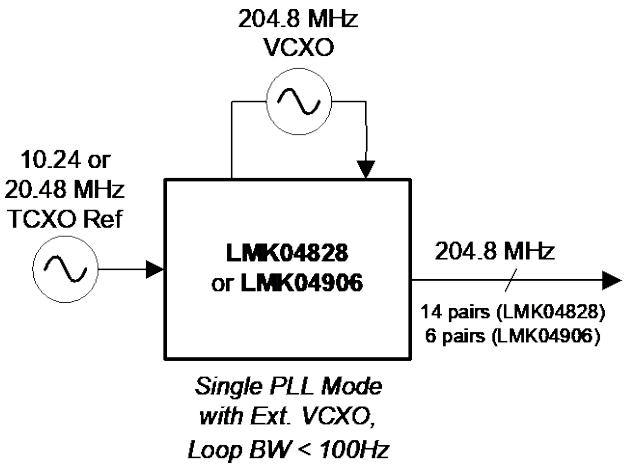


Figure 4 - Set-Up in Lab

- **PLL Simulation**

A single PLL configuration with TCXO & VCXO noise models is shown in Figure 5.

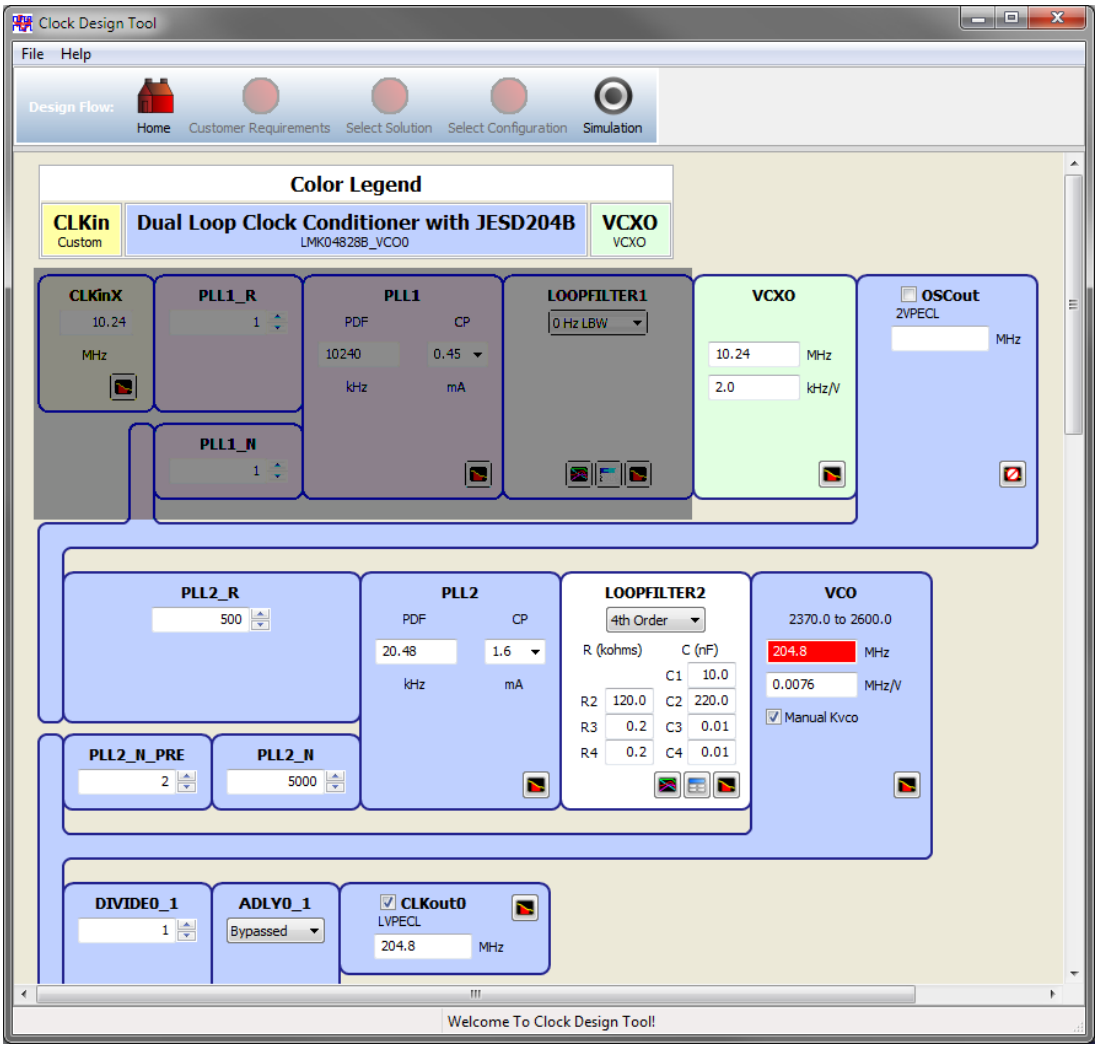


Figure 5 - Single PLL Configuration with TCXO & VCXO Noise Model

Temperature compensated crystal oscillator specification is shown in Figure 6.
We use Vectron's VT-820 as a simulation model (Figure 7).

Parameter	Symbol	Min.	Typ	Max	Units
Output Frequency	f_O	8		45	MHz
Supply Voltage,[1] (Ordering Option)	V_{DD}	+1.8, 2.8, +3.0 or +3.3			V
Supply Current, 8 to 19.999MHz 20.000 to 31.9999MHz 32.000 to 45.000MHz	I_{DD}			1.5 2.0 2.5	mA
Operating Temperature, (Ordering Option)	T_{OP}	0/55, -10/60, -20/70, -30/80, -30/85, -40/85			°C
Stability Over T_{OP}, (Ordering Option)		±0.5, ±1.0, ±1.5, ±2.0, ±2.5, ±3.0, ±3.5 ±4.0, ±5.0			ppm
Initial Accuracy[2], "No Adjust" Option				±1.0	ppm
Power Supply Stability, ±5% change				±0.2	ppm
Load Stability				±0.2	ppm
Aging				±1.0	ppm/yr
Pull Range, (Ordering Option)	TPR	±5, ±8, ±10, ±12, ±15			ppm
Control Voltage to reach Pull Range 1.8V option		0.5 0.3		2.5 1.5	V V
Control Voltage Impedance		500			Kohm
Output Level[3]	V_O p/p	0.8			V
Output Load				10K II 10pF	
Phase Noise, 10.000MHz 10Hz 100Hz 1kHz 10kHz 100kHz			 -91 -116 -137 -149 -150		dBc/Hz
Start Up Time				2	ms

Figure 6 - Vectron TCXO Datasheet

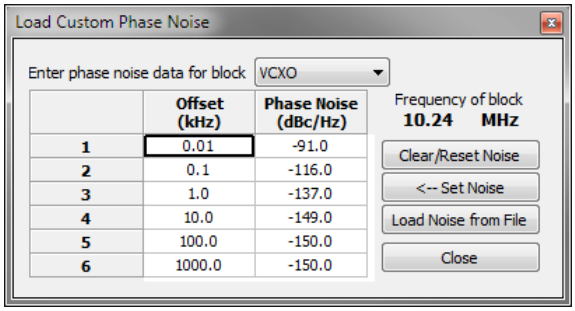


Figure 7 - TCXO Noise Model

Low noise and low jitter VCXO data are shown in Figure 8 and Figure 9. We use the RAKON: RVX7050M 204.800 MHz as simulation.

7.0 SSB Phase Noise

Parameter		Typ.	Max.	Unit	Test Condition / Description
a.	10Hz offset	-67		dBc/Hz	25°C
b.	100Hz offset	-97		dBc/Hz	25°C
c.	1kHz offset	-125		dBc/Hz	25°C
d.	10kHz offset	-145		dBc/Hz	25°C
e.	100kHz offset	-155		dBc/Hz	25°C
f.	1MHz offset	-155		dBc/Hz	25°C
g.	10MHz offset	-156		dBc/Hz	25°C

Figure 8 - RAKON VCXO Noise Model

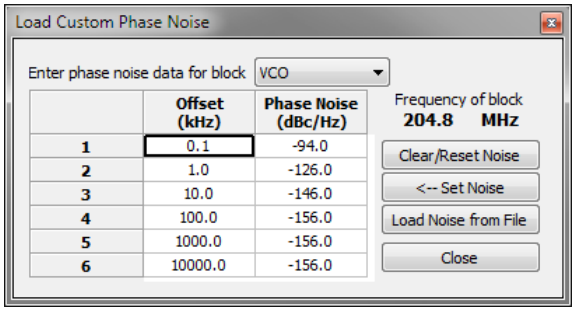


Figure 9 - VCXO Noise Model

PLL loop filter characteristics are shown in Figure 10.

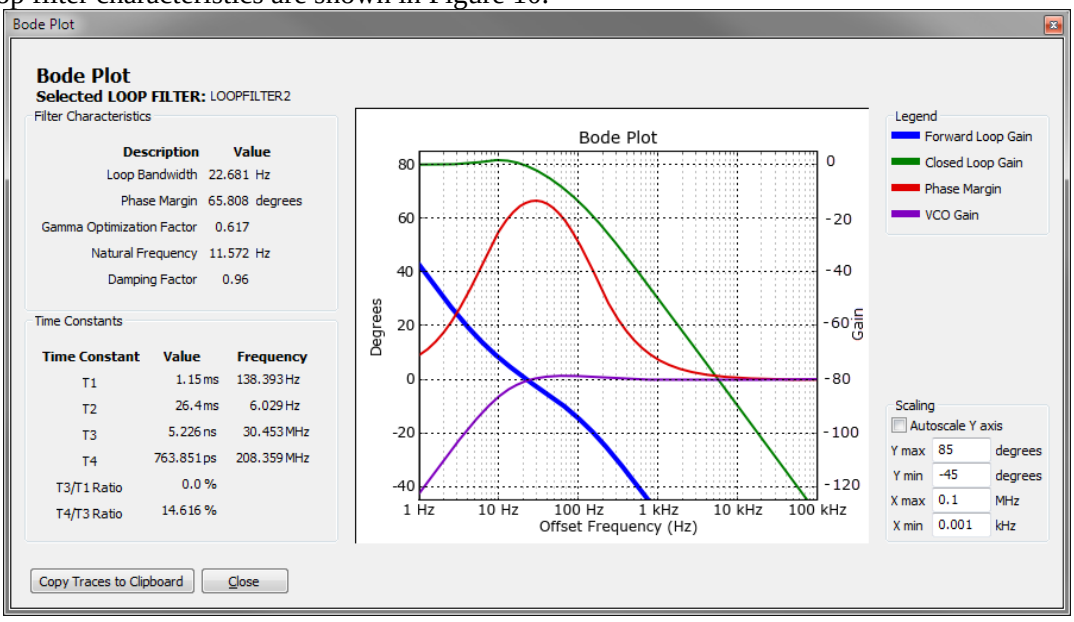


Figure 9 - PLL Loop Filter Characteristics

LVDS output phase noise / jitter are shown in Figure 11.

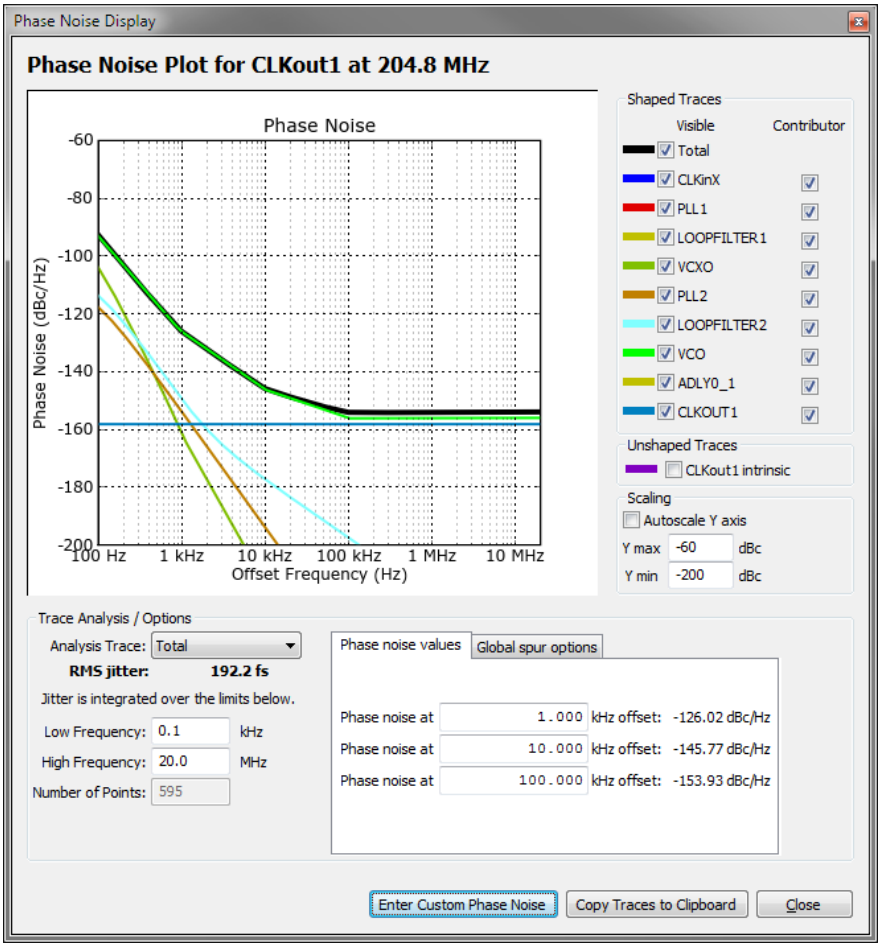
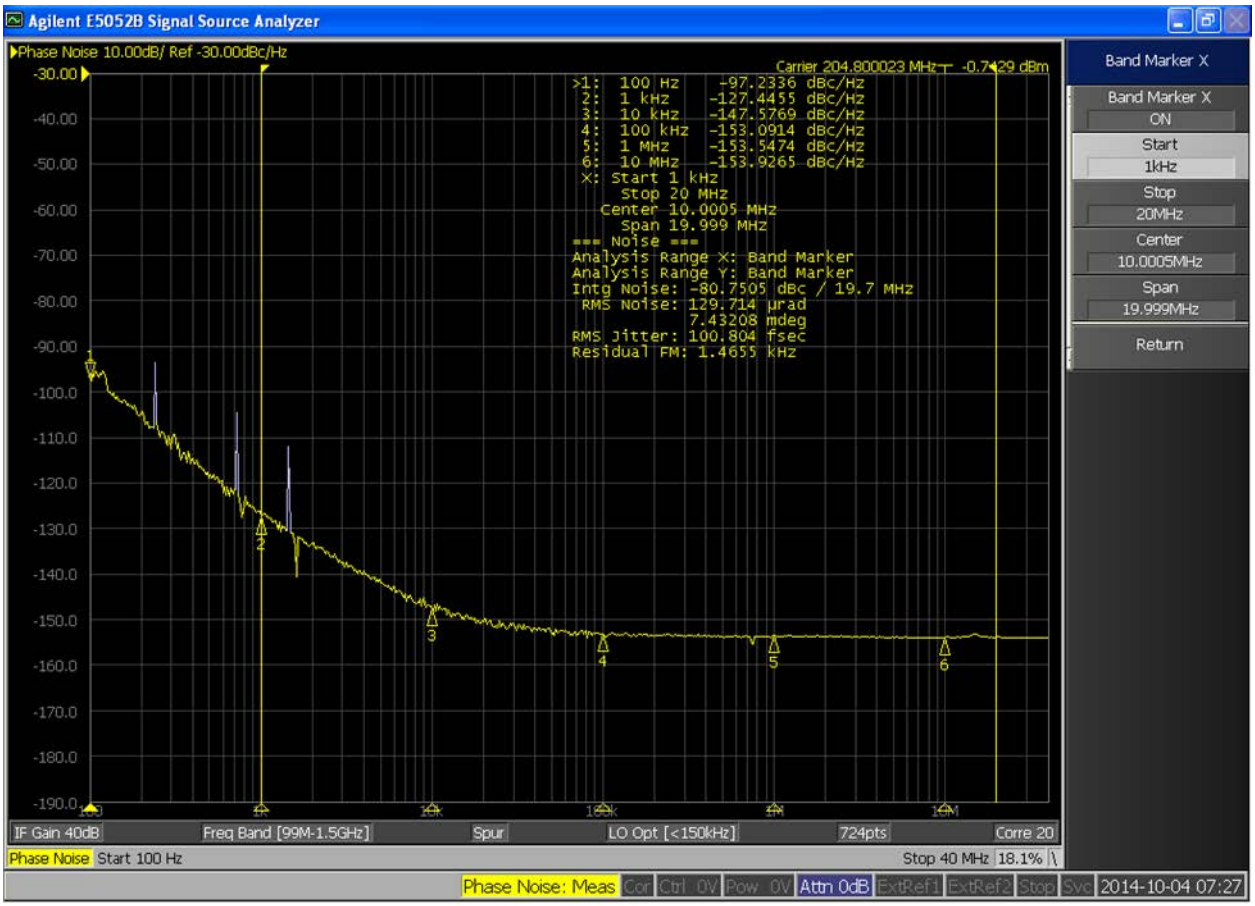


Figure 10 – PLL Phase Noise Simulation

- **Test Result**

Please see 204.8 MHz Output Phase Noise test results in Figure 12 and Figure 13, showing good margin over phase noise and integration jitter specification.



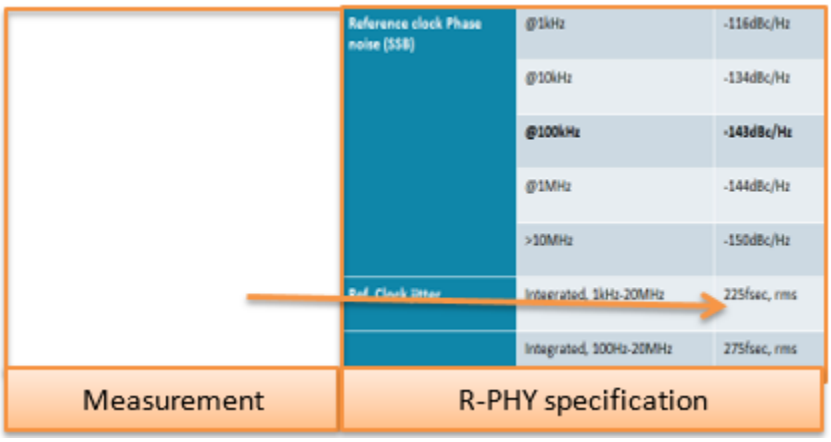


Figure 11 - PLL Phase Noise/Jitter (1 kHz to 20 MHz) test result

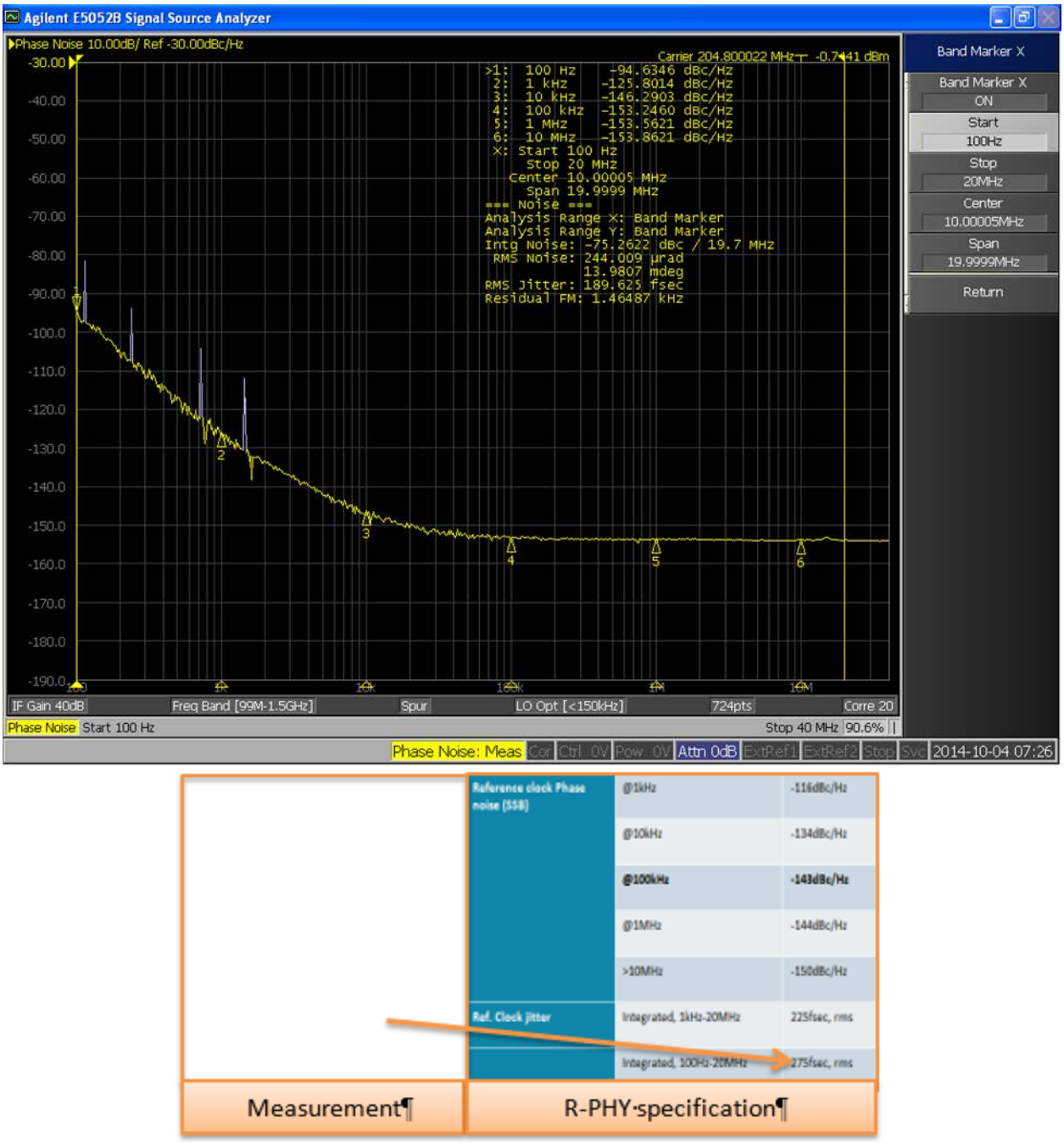


Figure 12 - PLL Phase Noise/Jitter (100 Hz to 20 MHz) test result

Solution 2: Frequency Synthesizer + VCXO

The ADF4002 frequency synthesizer is used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low-noise digital phase

frequency detector (PFD), a precision charge pump, a programmable reference divider and programmable N divider. The 14-bit reference counter (R counter), allows selectable REFIN frequencies at the PFD input.

- **Block Diagram**

A complete PLL can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). In addition, by programming R and N to 1, the device can be used as a standalone PFD and charge pump. See Figures 14 through 16 for block diagram, test configuration, and test results.

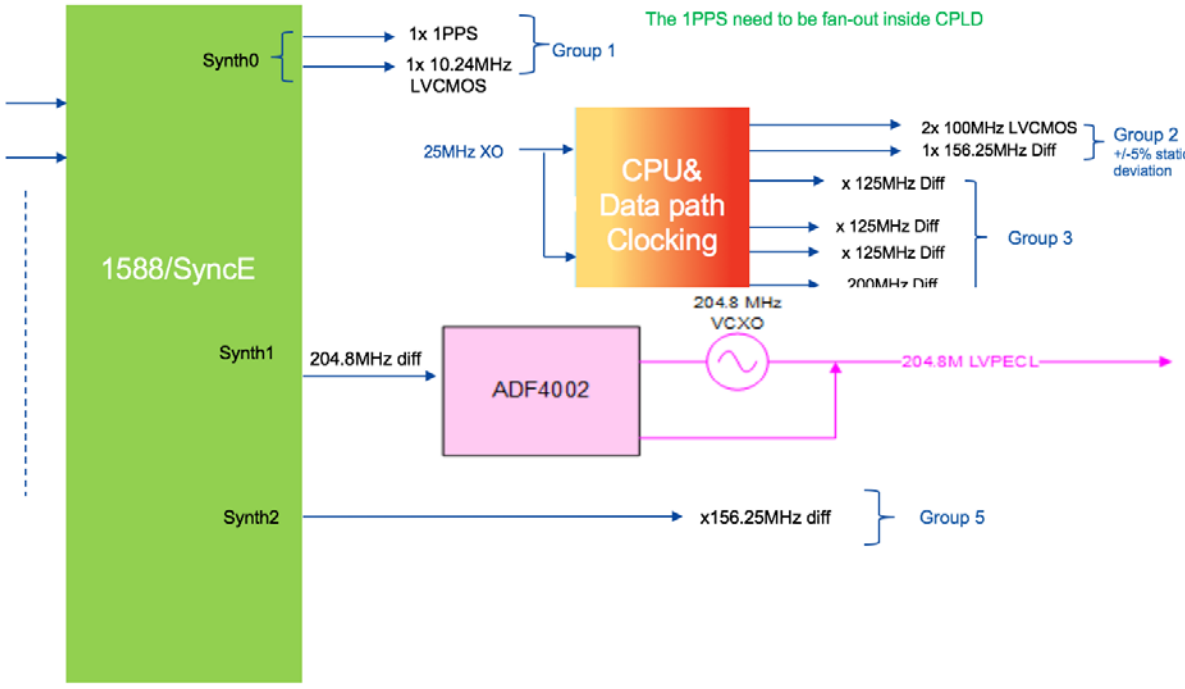


Figure 13 – ADF4002 with External VCXO

- **PLL Configuration**

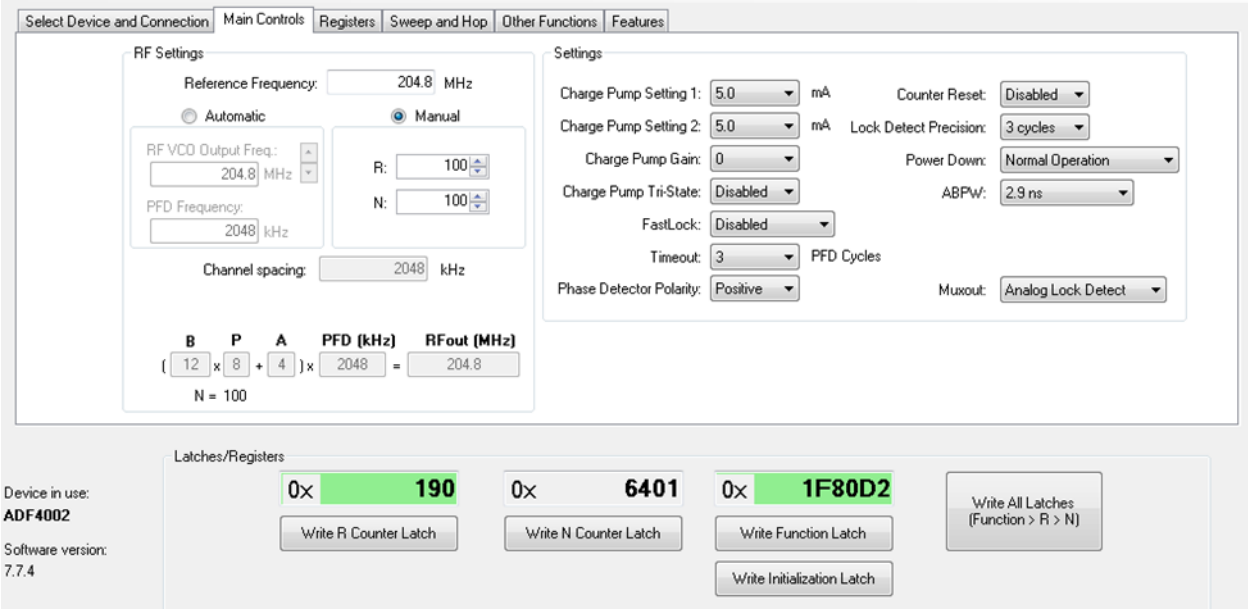


Figure 14 - ADF4002 Register Configuration

- **PHY3.1 Phase Noise@RPD Port Test Result**

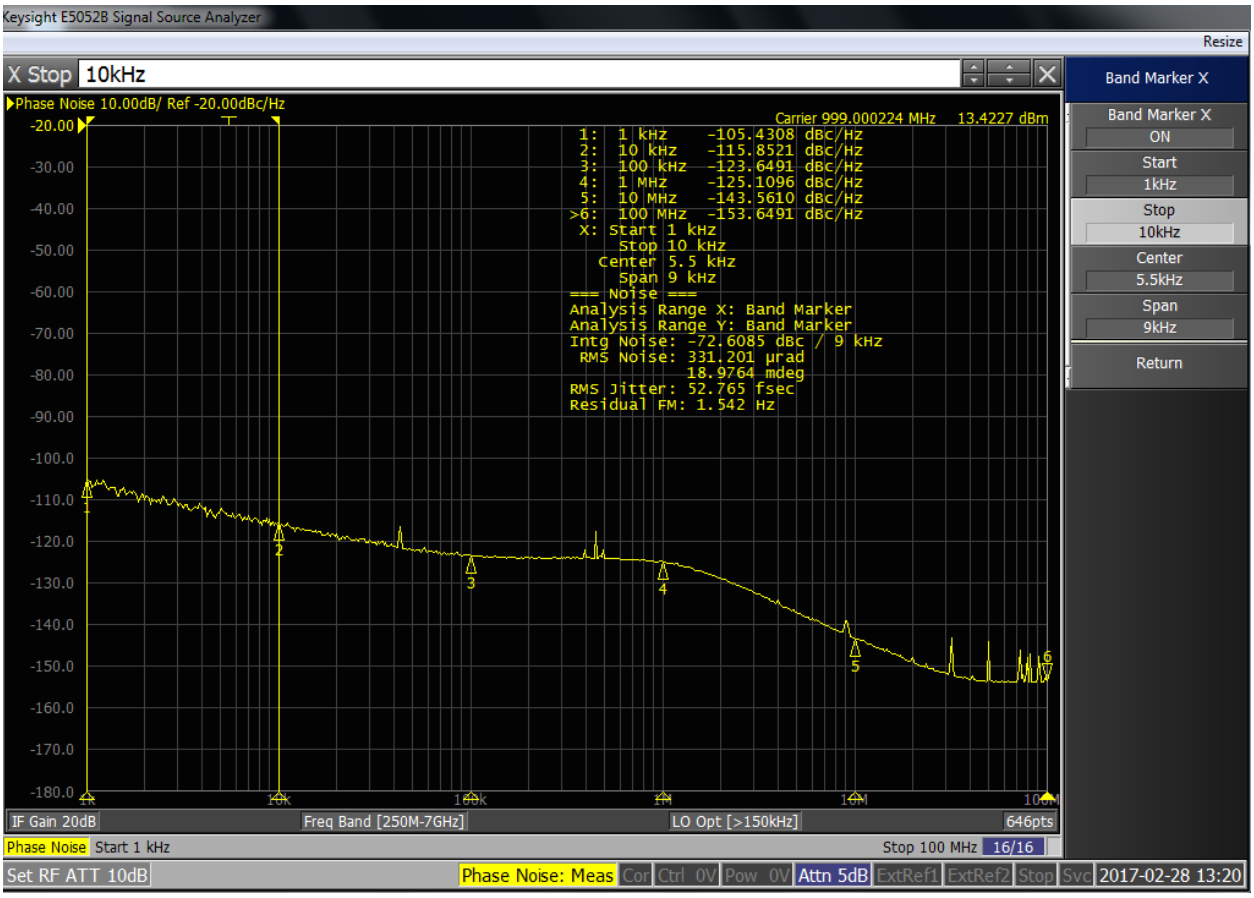


Figure 15 – PHY3.1 phase noise test @RPD RF port

Conclusion

This paper has highlighted best practices for DOCSIS 3.1 phase noise design in the remote PHY device with two clock solutions. It also proved that we can get good margin for not only phase noise but also for jitter performance considering the tough requirements from both PHY3.1 silicon chip and CableLabs PHY3.1 specification.

Abbreviations

A/D	analog-to-digital
ADC	analog-to-digital converter
CCAP	converged cable access platform
CW	continuous wave
D/A	digital-to-analog
DAC	digital-to-analog converter
dB	decibel
dBc	decibel carrier
DOCSIS	Data-Over-Cable Service Interface Specifications
DPLL	digital phase-locked loop
DRFI	[DOCSIS] Downstream Radio Frequency Interface [Specification]
FFT	fast Fourier transform
fs	femtosecond
GE	gigabit Ethernet
GHz	gigahertz
GSps	gigasamples per second
Hz	hertz
HW	hardware
IEEE	Institute of Electrical and Electronics Engineers
ISBE	International Society of Broadband Experts
kHz	kilohertz
LVDS	low voltage differential signaling
MHz	megahertz
OFDM	orthogonal frequency division multiplex
PFD	phase frequency detector
PHY	physical layer
PLL	phase-locked loop
ps	picosecond
RF	radio frequency
RPD	remote PHY device
RMS	root mean square
SCTE	Society of Cable Telecommunications Engineers
SNR	signal-to-noise ratio
SSB	single sideband
TCXO	temperature controlled crystal oscillator
VCO	voltage controlled oscillator
VCXO	voltage controlled crystal oscillator

Bibliography & References

DOCSIS 3.1 Physical Layer Specification CM-SP-PHYv3.1-I11-170510 TI 204.8 MHz test result
Cisco RPD HW design specification

